A 1.8 GHz to 2.1 GHz 0.25 µm CMOS Wideband LNA for a Multi-Standard Mobile Receiver

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Abstract-**A single-ended wideband low noise amplifier for a multi-standard (1.8 GHz to 2.1 GHz) mobile receiver has been designed and simulated in a 0.25 µm CMOS technology process. The circuit topology is based on inductively degenerated common source (IDCS). The enhancement for bandwidth was performed using inductive shunt-peaking that added more freedom to the circuit. Circuit simulation results shows a power gain of 23 dB, a noise figure of 0.6 dB with IIP3 and 1-dB compression point of – 5.1 dBm and –17.3 dBm respectively. The current consumption for this circuit is 9.5 mA with voltage supply of 2.5V.**

I. INTRODUCTION

At present, in the vast spectrum of mobile communications shows that different countries use different standards i.e. in U.S., Personal Communication System (PCS1900) is being used while in U.K., Global Standard for Mobile (GSM900) and Digital Communication System (DCS1800) is being implemented. In addition to those standards, Wide Code Division Multiple Access (WCDMA), also known as 3G or 3rd Generation System is increasingly being used in those countries and in other countries that implement the same systems. Therefore, the need for highly integrated solutions with low-cost technologies is critical to be able to use the same mobile terminal on a global scale.

The radio frequency (RF) front-end (of mobile device) consists of several integrated components such as a Low Noise Amplifier (LNA), mixer, Voltage Controlled Oscillator (VCO) etc. and it has to cover a large range of different carrier frequencies to satisfy the various standards. With respect to current solutions for multi-standard devices, multiple parallel LNA's are used to suffice the various standards, e.g. Qualcomm use different LNA in parallel to support standards such as GSM900, DCS1800, PCS1900, 3G etc. [1]. However this implementation is very area inefficient, costly and consumes unnecessary static power. Another technique is to use a wideband LNA that cover all those standards in one single circuit.

This paper describes the design of a wideband LNA for carrier frequency standards from 1800 to 2100 MHz (GSM + 3G). The topology used for LNA is inductively degenerated common source (IDCS) with bandwidth enhancements.

II. REVIEW OF WIDEBAND LNA TOPOLOGY

This section will highlight some of the topologies that are currently available in the research arena. Several approaches have been developed to attain a wideband design. One of them is implemented by [2] and its topology is shown in Fig. 1. This research is based on common-source topology with a common-drain feedback stage. The circuit is designed in differential mode. The design produced positive results with a very large bandwidth of a few gigahertzes. However, this design drives too much current (75 mA) while being area inefficient. Another approach is introduced in [3] and its topology is shown in Fig. 2. This wideband LNA has a single ended input and differential outputs. It produces a promising results but with quite high power consumption of 38 mW. In another example, the design is implemented using noise cancelling technique as described in [4] and its topology is shown in Fig. 3. It consumes the current of 14 mA from 2.5 V supply. Thus, with all of these examples, it shows that there are several approaches that can be used to design LNA that produce wide bandwidth. However, all the designs described are either designed for ultra wide band (UWB) communications or not for specific applications range from few MHz to several GHz. But none of them is specifically designed for personal mobile communication which consists of GSM and 3G standards.

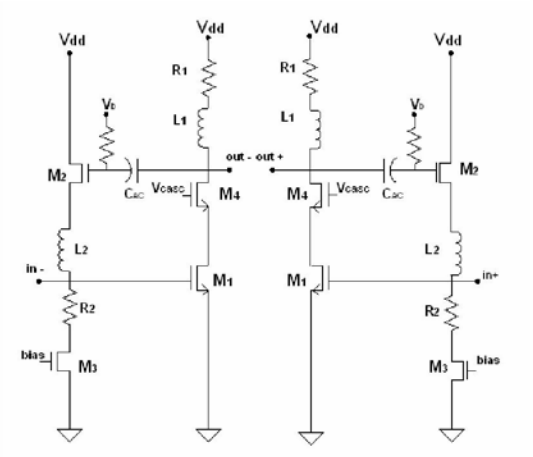

Fig. 1. Differential wideband LNA as highlighted in [2]

In the research work presented in this paper, the LNA design is specifically targeted for personal mobile

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communications standards that use IDCS as the topology. This topology was chosen because it provides good input matching and a low noise figure [5]. In addition, to the author's knowledge and from the available literature, the design introduced in this paper is believed to be the first wideband LNA design that is targeted for mobile communication specifically. The subsequent section will present details the design of the wideband IDCS LNA.

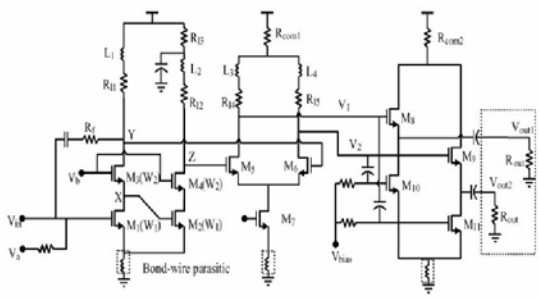

Fig. 2. Wideband CMOS LNA introduced in [3]

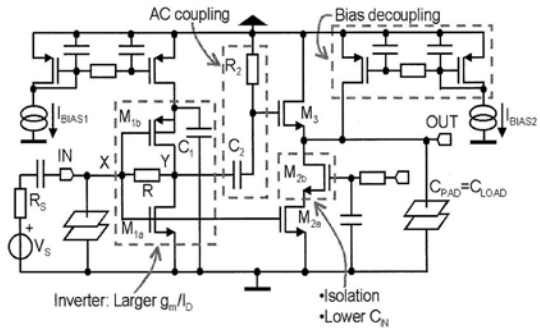

Fig. 3. Wideband LNA using noise cancelling as described in [4]

III. PROPOSED INDUCTIVELY DEGENERATED COMMON SOURCE LNA

The wideband LNA is designed as a single-ended LNA based on an inductively degenerated common source [5-6]. It follows the power-constrained noise figure (NF) condition in order to achieve low power and low noise with sufficient wide input-matching bandwidth [6].

Fig. 4 presents the schematic diagram of wideband IDCS LNA targeted to cover carrier frequency from 1800 to 2100 MHz. This range of frequency includes the GSM standards (DCS1800 and PCS1900) and 3G standards that cover frequency bands from 1800 to 2100 MHz. Thus, to accommodate such a frequency range from 1800 to 2100 MHz, a new frequency centre of 2 GHz was chosen. The input-matching bandwidth i.e., the frequency range that satisfies 20 log $|S_{11}| \leq -10$ dB was selected to be 0.4 GHz to accommodate any possible frequency variation [6].

The input impedance Z_{in} for the design is based on 50 Ω system using the following equation:

$$Z_{in} \approx s\left(L_g + L_s\right) + \frac{g_{m1}L_s}{C_{gs}} + \frac{1}{sC_{gs}} \quad (1)$$

where L_g is the gate inductor, L_s is the source inductor, C_{gs} is the gate-source capacitance and g_{m1} is the transconductance of input device M1.

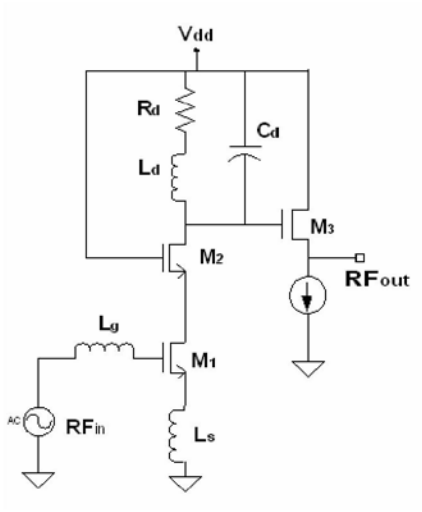

Fig. 4. Wideband IDCS LNA.

With respect to input matching, it follows the theory highlighted by [6] which gives the normalized matching bandwidth that sets the lower and upper limit of the total inductance of the inductors connected to the input transistor. To attain the flat and low NF over the chosen bandwidth based on the theory introduced, the size of transistor M1 and the inductances of L_g and L_s are set. Therefore, the cascode transistors M1 with M2 with L_g and L_s connected as in Fig. 4 set the input impedance and noise-matching simultaneously.

Transistor M2 is used for reducing the Miller effect. L_d and C_d function as tuned load and M3 act as a buffer. To add more freedom to the circuit in terms of gain control and bandwidth enhancement, inductive shunt-peaking is implemented in the circuit by connecting resistive load, R_d in series with an inductance, L_d [7]. Thus, voltage gain, A_v can be calculated as expressed in (2)

$$A_v = \frac{f\left(gm, C_{gs}\right) \bullet Z_{load}}{Z_{in}} \quad (2)$$

where $Z_{load} = R_d + sL_d$.

IV. SIMULATION RESULTS

The wideband IDCS LNA is designed using a 0.25 µm standard CMOS technology. Figures 5 to 9 illustrate the simulation results for the S-parameter, noise figure, third-order intercept point and 1 dB compression point (1-dB CP) respectively.

In Fig. 5, the input reflection coefficient (S11) of the LNA achieved is –23.8 dB while output reflection coefficient (S22) is –23 dB at peak frequency. As shown in Fig. 5, the input reflection coefficient remains under –10 dB which begins from 1.6 GHz and ends at 2.4 GHz. This yields twice the bandwidth acquired. It also indicates that the design for input impedance matching is acceptable and within expectation. However, for the output reflection coefficient, the bandwidth achieved follows the bandwidth set by the calculation which is from 1.8 GHz to 2.2 GHz. Therefore, S22 is not as superior as S11, but it is still within expectation.

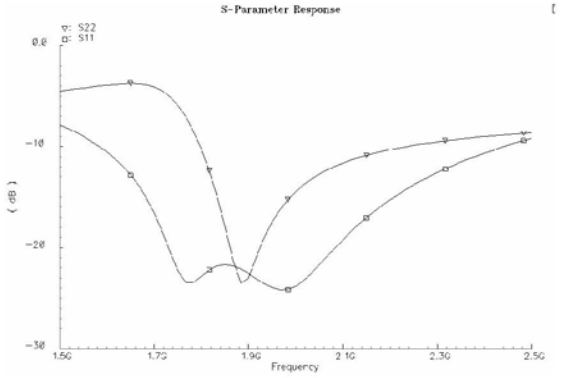

Fig. 5. Input and Output Reflection Coefficient.

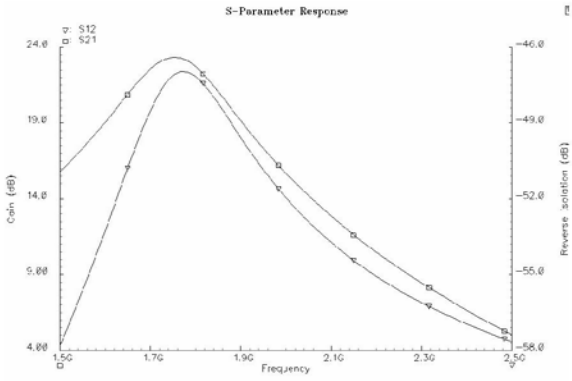

Fig. 6. Power Gain and Reverse Isolation.

Fig. 6 presents the S21 or power gain achieved in the simulation. The illustration indicates a value of 23 dB at peak and remains approximately at 10 to 23 dB along the design bandwidth. Fig. 6 also shows the reverse isolation or S12. The attained value is –47 dB and is believed to be a good reverse isolation as it exceeds the requirement that is typically –30 dB.

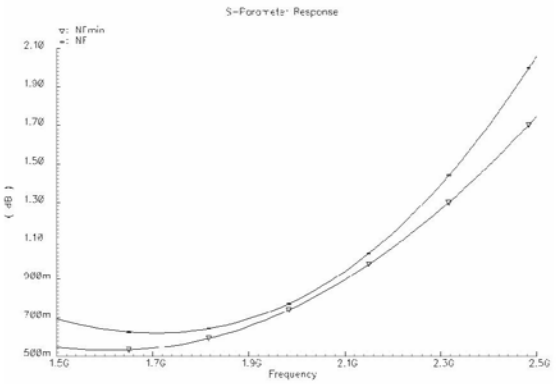

Fig. 7. Noise Figure.

Fig. 7 shows the noise figure of the LNA achieved in the simulation. It is quite flat over the band of interest and is about 0.6 dB at peak. This value is believed to be the lowest thus far achieved in the design of wideband LNA based on the IDCS topology. On the contrary, this value might be higher if the LNA enters fabrication which might be due to the process variation, parasitic values or other abnormalities during fabrication. Also shown in that figure is the minimum noise figure which is about 0.5 dB at peak frequency.

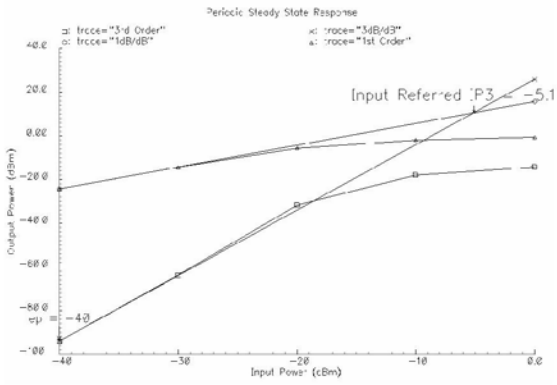

Fig. 8. Third-order Intercept Point.

To check for the linearity requirement, a two-tone test for third-order intercept point was performed on the LNA. The two tones were applied at frequencies of 2 GHz and 2.05 GHz respectively with equal power. The achieved third-order input intercept point or IIP3 is –5.1 dBm and is shown in Fig. 8. This value achieved is typically an acceptable

specification and represents the tradeoff between power consumption and linearity requirements. In other words, the design has been optimised to obtain the best IIP3 value with intention to consume the least amount of current in the circuit. In addition, transistor M3 limits the linearity of the circuit due to the gain which precedes it.

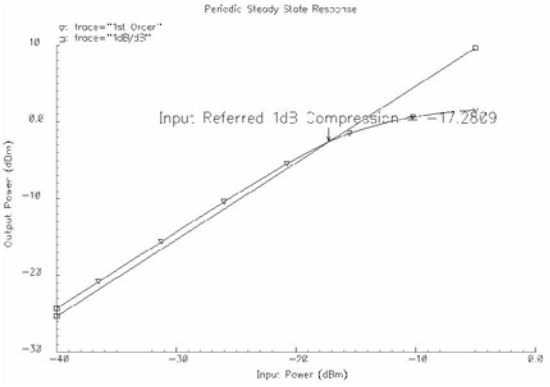

Fig. 9. 1 dB Compression Point.

Another measurement for linearity is the 1-dB CP. As shown in Fig. 9, the simulated 1-dB CP achieved is –17.3 dBm. Notice that the achieved value is typically an acceptable specification and is a tradeoff between power consumption and linearity requirements.

TABLE I
LNA PERFORMANCE SUMMARY

Parameter	This work 0.25 µm	[2] 0.18 µm	[6] 0.25 µm
Frequency (GHz)	2	2.45	5.467
Noise Figure (dB)	0.6	3.7	1.78
S21 (dB)	23	13.1	23
S11 (dB)	–23.8	– 4.8	–22
S22 (dB)	–23	–16	–17
S12 (dB)	–47	n/a	–40
IIP3 (dBm)	–5.1	–4.7	n/a
1-dB CP (dBm)	–17.3	–15.2	n/a
Supply Voltage (V)	2.5	n/a	2.5
Power Con. (mW)	23.75	75	30

Table I gives the summary performance of the LNA achieved in the simulation. It also shows some of the other research results which have been obtained recently. In comparison in term of power, the LNA presented in this paper consumes less power consumption which is 23.75 mW compared to [2] and [6] which is 75 mW and 30 mW respectively. This result is due to the intention to make the LNA power efficient. In term of the noise figure, the circuit designed is very low in noise performance compared to [2] which is 3.7 dB and 1.78 dB for [6]. The rest of the parameters are as shown in the table.

V. CONCLUSION

A single-ended wideband LNA for a multi-standard mobile receiver has been presented and discussed. The circuit topology used together with bandwidth enhancement shows better performance than several other topologies and meet the specification for wideband applications for personal mobile communications. The presented design was implemented using a 0.25µm CMOS technology process. Simulation results show promising performance in terms of the noise figure, gain, input and output impedance matching. However the linearity of the system that represented by IIP3 and 1-dB compression point achieved is just a typical. To enhance the linearity requirement, we can increase the current consumption but it increases the power consumption of the circuit. Thus, future work is currently being undertaken to improve the linearity of this circuit. Finally, the conclusion of this work shows that the design of wideband LNA can be achieved using IDCS which is typically used for narrowband systems.

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