Design and Investigation of Low-Power Linear-In-Decibel S-Band Power Detector

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Master of Engineering (Research)

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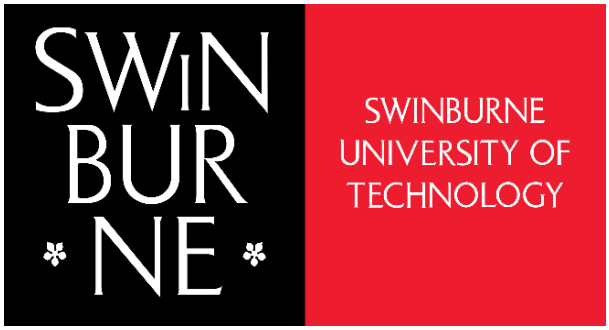

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Abstract

Microwave power detection has gained major significance as most electronic devices communicate through radio frequency (RF). According to Cisco's latest networking Index (VNI) report, by 2022, the global networked devices and connections will reach 28.5 billion, representing an increase of more than 10%. Henceforth, controlling the specified power levels limits is crucial to accomplish the range and reliability in a multi-user environment. Recent advancements in new technology processes such as CMOS technologies have enhanced researchers' interest in RF power detectors.

This research aims to design a low-power linear-in-decibel RF power detector using a 180 nm standard CMOS process. The RF power detector targets S-band frequency range (2 GHz to 4 GHz) applications in wireless communication and as sensing devices in the agriculture sector, where low-power consumption, wide dynamic range, and high sensitivity are required. This research also explores various design considerations for low-power linear-in-decibel RF power detectors and provides an in-depth analysis on enhancing their sensitivity at low input signal power.

The proposed linear-in-decibel RF power detector is designed and simulated using Keysight Advanced Design System (ADS) with 180 nm CMOS process parameters. The RF power detector comprises an RMS power detector, a DC offset compensation circuit, and a five-stage successive detection logarithmic amplifier. MOSFETS square-law characteristic in the saturation region is exploited to perform power detection. A cascode circuit configuration with a current-source-load operating as an RMS power detector is placed before the logarithmic amplifier to improve the sensitivity of the RF power detector. Considering that the input signal of the successive detection logarithmic amplifier is a DC voltage, no rectifier was required. Hence, power dissipation and chip area are reduced considerably. Therefore, the efficiency and suitability of the proposed RF power detector for low power applications are enhanced. The RF power detector simulation results demonstrate that the power can detect power from -60 dBm to 0 dBm with an error of ±2 dB. The power detector operating frequency is from 2 GHz to 4 GHz, and the dynamic range of 40 dB and 30 dB is simulated at 2 GHz and 4 GHz, respectively. The simulation results also show that the preceding RMS detector enhances the RF power detector sensitivity by 20 dB. The total power consumption is 0.610 mW with a supply voltage of 1.8 V.

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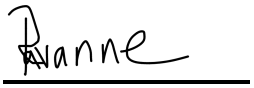
Declaration

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university, and to the best of my knowledge, contains no material previously published or written by another person, except where due reference is made in the text of the thesis. Work-based on joint research or publications in this thesis fully acknowledges the relative contributions of the respective authors or workers.

Signature	:	
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Design and Analysis of a Practical RMS Power Detector Using Power MOSFET, IEEE IEMCON (2021 IEEE 12th Annual Information Technology, Electronics, and Mobile Communication Conference) [Status: Accepted (Presented and in Press)]

Table of Contents

List of Figures

List of Tables

Lists of Abbreviation

AC – Alternating-Current

ADC – Analog-to-Digital Converter

ADS – Advanced Design System

ADSL - Asymmetric Digital Subscriber Line

AGC - Automatic-Gain-Control

ALC – Automatic Level Control

AM – Amplitude Modulation

ATSC - Advanced Television Systems Committee

AVG - Average

BGR - Bandgap Reference

BiCMOS – Bipolar Complementary Metal-Oxide-Semiconductor

BJT - Bipolar Junction Transistor

CAD – Computer-Aided Design

CATV - Community Antenna Television

CMFB - Common Mode Feedback

CMOS - Complementary Metal-Oxide-Semiconductor

CMRR - Common Mode Rejection Ratio

COFDM - Coded Orthogonal Frequency Division Multiplexing

CTAT - Complementary to Absolute Temperature

D2S - Differential to Single-Ended Amplifier

DC – Direct-Current

DTV-T - Digital Video Broadcasting Terrestrial

GAs - Gain Amplifiers

GBW - Gain-Bandwidth Product

GSM - Global System for Mobiles

I/O – Input/Output

ICs – Integrated Circuits

IEEE - Institute of Electrical and Electronics Engineers

IF – Intermediate Frequency

IoT - Internet of Things

LNA – Low Noise Amplifier

LPF – Low-Pass-Filter

MC – Monte Carlo

MOSFETs - Metal–Oxide–Semiconductor Field-Effect Transistor

MPT – Microwave Power Transfer

MTL - MOSFETs Translinear Loop

NF – Noise Figure

NMOS - N-Channel Metal-Oxide Semiconductor

PAR – Peak-Average-Ratio

PDKs - Process Development Kits

PSSR – Power Supply Rejection Ratio

PTAT - Proportional to Absolute Temperature

PTM - Predictive Technology Model

PWL – Piecewise-Linear-Approximation

QAM - Quadrature Amplitude Modulation

RF – Radio- Frequency

RMS – Root-Mean-Square

RSSI - Received Signal Strength Indicators

SCL – Scattering Limited

SDLA – Successive Detection Logarithmic Amplifier

SNR – Signal-to-Noise Ratio

SQRs - Squaring Cells

TC – Temperature Coefficient

TIA - Trans-Impedance Amplifier

VNI - Visual Networking Index

VSWR - Voltage Standing Wave Ratio

WCDMA - Wideband Code Division Multiple Access

Lists of Symbols

C_{ox} - Capacitance per Unit Area

q – Thermal voltage

Q -Quality Factor

W – Watt

μ_n - Average Electron Mobility

Chapter 1

Introduction

This thesis explores the design and investigation of RF power detectors for application in the S-band frequency range. The main focus is on linear-in-decibel RF power detectors and their implementation using CMOS technology processes. The critical parameters such as dynamic range, operating frequency, sensitivity, and power consumption are investigated thoroughly for an efficient and robust design. This thesis also investigates the noise characteristics of the RF power detector and their impacts on design considerations. This chapter provides a comprehensive research background, followed by the problem statements and the research objectives for this thesis. Finally, the thesis organization is given at the end of the chapter.

1.1. Research Background

The rapid growth of modern technology involving radio frequency (RF) and microwave engineering in the agricultural and telecommunication industries has raised awareness to develop power detectors with high accuracy and low power consumption. Power detectors are mainly used to detect the power of a transmitted signal.

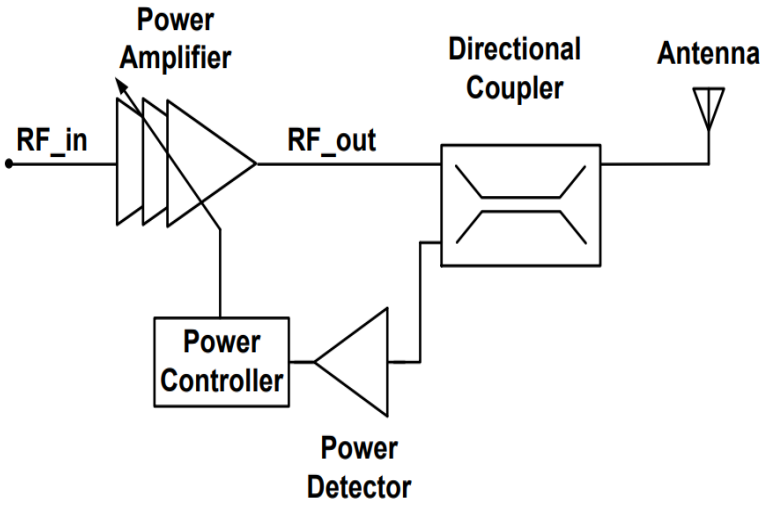

Figure 1: Conventional RMS power detector in an RF transmitter (Wang et al. 2015).

RF power detectors are involved in various applications, including integrated circuit tests and measurements, wireless communications, and automatic-gain-control circuits (AGC) to monitor

signal power levels. Power detectors are utilized as If (RSSI) to adjust the VNI/RF signal's gain via an AGC circuit (Wang et al. 2015).

They are also used in mobile terminals to monitor the transmitted power, thereby optimizing power consumption. These transmitted and received power must be controlled fast and accurately to comply with government regulations with minimum interference and optimum power consumption. Optimum power consumption is a critical power detector parameter since most electronic devices utilize batteries with finite power. Thus, optimizing power consumption will increase the battery life allowing portable devices to operate for a longer period. Nowadays, since consumers are using their devices more extensively, minimum power dissipation is the main focus. In addition, from Cisco's latest networking Index (VNI) report, by 2022, the global networked devices and connections will reach 28.5 billion, representing an increase of more than 10% (Cisco 2018). Thus, controlling the power levels in the specified limit is significant to achieve reach and accuracy.

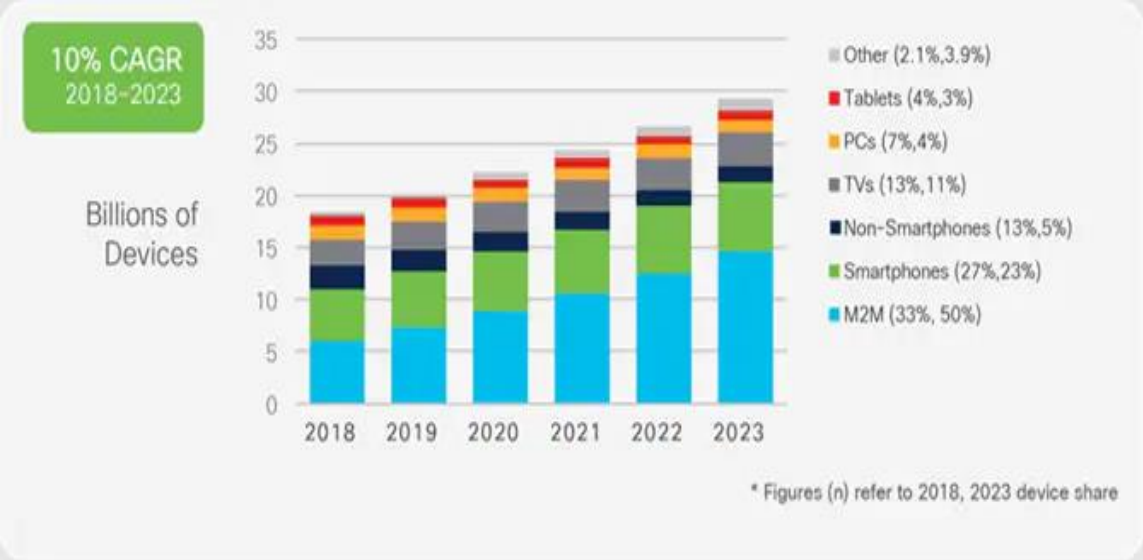

Figure 2: Global Internet user growth (Cisco 2020).

Consequently, the market demand for low-power and high dynamic range RF power detectors has experienced an exponential increase in recent years. New design techniques have emerged to address current problems and enhanced RF power detectors' performance metrics, such as operating frequency, dynamic range, sensitivity, and power consumption. There has already been substantial research in developing accurate and robust power detectors that operate in various

frequency ranges. One of the simplest power detectors in the market for many years is fabricated using the Schottky diode. Even though the Schottky diode operates well at high frequencies, its application is limited as it has a large parasitic capacitance which decreases its frequency range. From literature (Milanovic et al. 1996), it was confirmed that the accuracy of the Schottky diode for the small device was restricted. Figure 3 shows Simplified diagram of the diode detector circuit employed by Milanovic et al.

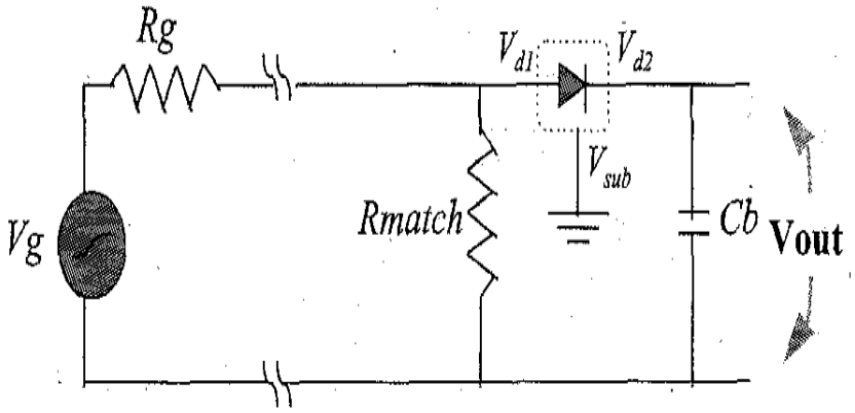

Figure 3: Simplified diagram of the diode detector circuit (Milanovic et al. 1996).

This was because the parasitic capacitances caused by the pads and metal lines could not be disregarded and, in reality, dominated the measurements. Another popular power detector circuit configuration is the bipolar junction transistor. This technology has quite promising advantages, but its production cost is high, making it inadequate for mass production. Besides, both the Schottky diode and the bipolar junction parameters deteriorate over temperature. Other examples of RF power detectors design techniques include thermal detection (Brush 2007; Kitchin & Counts 1983), bipolar junction transistors (BJT) (Zhang et al. 2006), current-mode computational circuits (Valdes-Garcia et al. 2008), or metal-oxide-semiconductor field-effect transistor (Sakphrom & Thanachayanont 2012; Xu et al. 2014; Zhou & Chia 2008).

In addition to application requirements, design methodologies, and performance metrics, the technology utilized to fabricate power detectors is also crucial. Various technological processes are currently being used in the market, such as BiCMOS, CMOS, and III-V technologies, to improve design parameters, addressing particular application requirements. BiCMOS technology offers excellent noise performance and ensures high I/O speed and switching. BiCMOS also achieves lower power consumption than bipolar technologies and improved speed over CMOS

technology (Zhou & Chia 2008). However, the process complexity of BiCMOS results in a higher cost and longer fabrication cycle time compared to CMOS technology (Harame 1997). III-V technologies offer higher electron mobility compared to silicon, making them appropriate for low-power and high-speed applications (Shah & Pei 1989). Though BiCMOS and III-V technologies present superior performance presently, CMOS technology is the preferred option to fabricate ICs due to its ultra-low power consumption, higher packing density, and low cost. In addition to that, CMOS technologies provide higher ease of integration for digital and analogue functions on the same chip. CMOS technology also has a higher density for digital operations and a high slew rate and gain for analogue functions (Zimmer 1984). This current advancement of microwave integrated circuit performance in standard CMOS technologies in terms of ease of integration, power consumption, and cost has made the design of microwave power detectors using CMOS a compelling choice. Therefore, CMOS technology is the preferred option to fabricate power detectors because its different advantages make it suitable for mass production (Qayyum & Negra 2017a).

1.2. Research Problems

Radio frequency and microwave applications in the S-band frequency have increased exponentially, increasing the demand for accurate power detectors to track signal power accurately. Although power detectors are employed in multiple applications, there is still a need for affordable, low-power, and accurate power detectors. This is mainly because Schottky diodes are unavailable in many advanced low-cost processes, and so is its alternative, the bipolar junction (Zhang, Fusco & Zhang 2012). Recent research using cheaper power detectors showed weak readings riddled with noise (Vithanawasam, Then & Su 2019). Then again, any power detector which is of better quality is too expensive. Furthermore, previous research has also established that high dynamic range and linear-in-decibel power detectors are most suitable for precise RF control, sensors, and wireless communications; however, those designs usually involve high power consumption (Hao et al. 2019; Lee, Song & Nam 2009; Lee, Song & Nam 2008; Wang et al. 2013). The high power consumption is mainly due to the cascaded stages of limiting amplifiers and rectifiers. Henceforth, the market demands a high dynamic range low-power linear-in decibel RF power detector for RF control and wireless communications applications. Moreover, currently, there is a lack of research for power detectors in the S-band frequency range, although it has various applications. For example, the S-band frequency is

suitable because most microwave ring resonators for agricultural applications operate in frequencies ranging between 2 GHz and 4 GHz (Chauhan, Tiwari & Singh 2017).

In order to address these challenges, an accurate power detector that operates in the S-band frequency needs to be designed. This power detector should have a low power consumption with enhanced power measurement accuracy. Consequently, CMOS technology stands out as the preferred option due to its low power leakage. Therefore, this study focuses on designing and investigating a low-power linear-in-decibel RF power detector for application in the S-band frequency. The research questions for this project are as follows:

I. What is the best RF power detector design employed for wireless communication applications using CMOS technology processes?
II. What are the design considerations to optimize power consumption of linear-in-decibel wide dynamic range RF power detectors?
III. How does noise affect the accuracy of RF power detectors and its impact on design considerations?
IV. What are the design techniques employed to improve the sensitivity of RF power detectors?

1.3. Research Goals and Objectives

This study investigates various design methods to reduce the high power consumption of logarithmic amplifiers without reducing their accuracy. This study also investigates potential design methodologies which enhance the sensitivity of logarithmic RF power detectors. High sensitivity is a critical design parameter for RF power detectors employed as precise measuring devices or sensors. Thus, this study focuses on designing and implementing a linear-in-decibel RF power detector using CMOS technology processes. The research objectives set to solve the research problems stated in sub-section 1.2 and thus providing an RF power detector using CMOS technology for applications in the S-band frequency range are as follows:

i. <u>To investigate and design a low-power linear-in-decibel RF power detector capable of reading up to 4 GHz.</u>

   The first objective is to develop a possible schematic for our new RF power detector that fulfils all the requirements per design specifications. CMOS technology will be

used to implement the power detector due to the low power consumption. Furthermore, the power detector must read frequency up to 4 GHz.

ii. To analyse the characteristics and critical parameters of linear-in-decibel RF power detectors via CMOS technology.

To verify the performance of the design, all the power detector characteristics, such as its input-output characteristics, dynamic range, linearity, sensitivity, and power consumption, will be analysed. The transfer characteristic of the RF power detector must also be analysed to establish a satisfactory output reading. The critical parameters of the RF power detector should match design specifications.

iii. Analyze the noise characteristics of the linear-in-decibel RF power detector.

In the case of RF power detectors designed using logarithmic amplifiers with a wide dynamic range, noise could result in severe fault and inaccuracy at the output. Furthermore, since noise establishes the minimum detectable signal of the RF power detector, thus its sensitivity, it is crucial to investigate the noise characteristics of the RF power detector.

1.4. Research Scope

The evolution of new integrated circuit design architecture and applications bring about new challenges to chip design. With a continuous boost in demand for smaller chip designs, low power consumption has become fundamental. The increased microwave applications due to smart technologies' current advancement justify the need for more accurate and affordable power detectors with low power consumptions for precise RF control. Recently, in literature, a new technique for designing linear-in-decibel RF power was proposed. This technique employs an RMS power detector for power detection and a logarithmic amplifier, further amplifying the signal to generate linear-in-dB output (Thanachayanont 2015). The rectifier was omitted since the logarithmic amplifier's input is a DC voltage, reducing power dissipation. Considering that this technique proved to be promising, we emphasize our research based on this new technique. This present investigation's findings aim to provide a low-power and accurate power detector within the semiconductor industry, particularly wireless communication. A stepwise analysis will be provided to investigate the design implementation feasibility. After system-level verification,

the design method shall be subjected to implementation and simulation at the circuit level. The simulation results will then establish the performance accuracy of the designed RF power detector.

1.5. Thesis Organization

This thesis is structured in the following six chapters:

Chapter 1 is an introduction chapter which provides research background, problem statements, research goals and objectives as well as the research scope.

Chapter 2 provides comprehensive review of microwave power detectors. Various published microwave power detection fundamentals and their operating conditions were reviewed. The RF power detector critical operating parameters and working principles of MOSFET were also further analyzed. A review of the different microwave power detectors design strategies using the standard CMOS process and analysis of the measurement is also presented. Issues of the different methodologies are raised, and comparisons are drawn.

Chapter 3 provides the design specification of the proposed RF power detector to meet applications requirement. This chapter also presents the CMOS characterization for the particular CMOS technology employed in this study to understand its fundamental properties better.

Chapter 4 presents the proposed methodology for designing the low-power linear-in-decibel RF power detector, including specifications, description of each functional block, mathematical analysis, and the circuit architecture. This chapter also presents a theoretical analysis regarding the operation of the logarithmic amplifier and other crucial functional blocks.

Chapter 5 presents the RF power detector simulation results thoroughly. A detailed discussion of simulation results is provided. This chapter also presents a comparison of the critical parameters of the proposed RF power detector and existing RF power detectors found in the existing literature.

Lastly, the conclusion based on the results and recommendations is presented in chapter 6.

Chapter 2

Literature Review

This chapter reviews the evolution of RF power detector design in CMOS technology found in the existing literature. Firstly, the fundamentals of power measurement and the importance of precise power detection are highlighted. The critical performance metrics of the RF power detector and its impact on the circuit architecture are also detailed. MOSFET'S characteristics in the different inversion regions and MOSFET short-channel effects are also described. This chapter will then delve into the various design techniques for power detectors in recent years and analyze their advantages and limitations. Different circuit implementation and their relationship with the performance metrics are discussed thoroughly. A critical review of the various RF power detectors circuit implementations is reported at the end of this chapter.

2.1. Fundamentals of RF Power Detection

The exponential increase of internet of things (IoT) devices has led to more restrictions imposed by agencies to measure the output power and prevent interference accurately. For instance, power levels must stay within the assigned range to function accurately in a multi-user environment. Power is preferred because its range is defined relative to the thermal noise floor (Cowles 2004). Thermal noise is proportional to bandwidth and absolute temperature but independent of impedance and frequency (White 2003). Two methods employed to measure the microwave power signal level are Root-Mean-Square (RMS) value and Peak value (Calvo & Pilotte 2006). Peak detection power detectors are used for constant envelope modulated signal, and RMS detectors are more accurate for microwave signal measurement. RMS detector generally involves square law detectors or thermal detectors with the advantages of better accuracy and wider bandwidth. Square law detectors utilize the attributes of semiconductor components to convert an input voltage into a signal proportional to the RF power (Thanachayanont 2015). Power expressed in Watts (W), most commonly used in measurement, is given by the measured RMS voltage and the impedance R,

$$P_{avg} = \frac{V^2_{RMS}}{R} [W] \qquad (2.1)$$

Root-Mean-Squared (RMS), also referred to as the heating or effective value of alternating current (AC), is equivalent to a DC voltage that would produce a similar heat generation as in an AC voltage applied to that same resistor. Its value can be expressed as

$$V_{RMS} = \sqrt{\frac{1}{T}\int V(t)^2\, dt} \qquad (2.2)$$

From equation (2.2), the average power is independent of the signal's waveform in the time domain. RMS voltage is the traditional way of measuring average power; however, signals expressed in absolute power levels are preferred for power detection applications. The impedance level relates to the RMS voltage and power level: thus, it is essential to specify the system's load impedance before comparing dBV and dBm (Nash 1999). As such, for an RF impedance of 50 Ω, the expression becomes

$$P_{avg}[dBm] \approx V_{RMS}[dBV] + 13[\text{dB}] \qquad (2.3)$$

Modern multiplexing and modulation methods in communication systems have led to complex signals with time-varying phase-amplitude. The Peak-to-Average Ratio (PAR) captures the variations of those time-varying signals that vary for different types of signals (Cowles 2004). Table 1 shows the PAR for different signals. Most measurement methods respond to some average instead of V_{rms}, leading to distinct readings for signals with different PARs but the same power.

Table 1: Par for different signals (Cowles 2004)

Sine wave	0 dB	50-850 MHz CATV (QAM)	12 dB
Gaussian Noise	9-12 dB	WCDMA (16 channel)	10 dB
ADSL (DMT)	15 dB	802.11a (52 carriers)	10 dB
Square wave/ DC	0 dB	ATSC (8-VSB)	10 dB
GSM/EDGE	0/3.2 dB	DTV-T (COFDM)	9.5 dB

Contrary to RMS peak detectors, peak detection output voltage changes with PAR, generating inaccuracy for a signal with high PAR values (Cowles 2004). For instance, depending on the signal complexity and impact of PAR on the signal, RMS or other non-RMS methods of power detection are chosen to measure power accurately.

2.2. Parameters

Power detector circuit configurations and design specifications depend on the performance parameters established for specific applications. The most critical performance parameters for power detector design and implementation are described in this section.

2.2.1. Operating Frequency

A consistent response is necessary over the frequency of operation. Two important parameters are required to accomplish this: the input impedance matching and the gain variation of the power detector against frequency (Genest et al. 2004). Input matching networks are circuitry connected between a load and source that ensures maximum power transfer to the load, thus, guaranteeing low Voltage Standing Wave Ratio (VSWR) (Yarman 2010). These two parameters simplify the design and maintain extremely low variation over the frequency of operation.

2.2.2. Sensitivity

Power detector sensitivity relates to the system's capability to obtain usable information from a low input signal (Genest et al. 2004). The minimum output signal level of the power should be lower than the minimum input signal level. Sensitivity is enhanced with an increased gain of the power detector; however, the power detector's saturation by gain degrades sensitivity. Sensitivity is very dependent on the input matching network of the system, and it affects the linearity of the power detector (Wei, Qayyum & Negra 2016).

2.2.3. Dynamic Range

Dynamic Range is the log-conformance within which the power detector satisfies the accuracy level over all operating conditions. Log-conformance is the ripple error arising from the difference between the power detector measured and ideal transfer characteristics (Muijs et al. 2013). The conventional value of log conformance is ±2 dB, even though smaller values such as ±1 dB and ±0.5 dB are acceptable (Cowles 2004). It is often employed to define the accuracy of logarithmic power detectors. A power detector with a larger dynamic range offers greater flexibility for selection with various system components, i.e., directional coupler (Nash 1999). As such, power detectors with a larger dynamic range are suitable for multiple applications.

2.2.4. Power Consumption

With the continuous downscaling of semiconductors, power consumption has gained major design significance comparable to performance and area (Thanachayanont 2015). Power consumption is a crucial design parameter as it impacts weight, cost, and size, and it establishes

the electrical and thermal limits of the designs. Furthermore, there is a reliability issue at high power consumption. High power systems that operate at high temperatures can cause silicon failures (Pedram 1996). From an environmental perspective, low-power electronic devices are preferred because lower electricity consumption lessens the global ecological impact.

2.3. MOSFET Principle of Operation

RMS power detectors perform RF power detection by exploiting MOSFET square-law characteristics in the saturation region. Nonetheless, within the saturation region, MOSFETs may be biased into three inversion regions: the weak inversion, moderate inversion, and strong inversion regions, each having distinct fundamental advantages. The strong inversion region is achieved when the MOSFET gate to source voltage is raised to a level where the drain current is much lower than the drift current. In contrast to the strong inversion region, the diffusion and drift components are similar in the moderate inversion region. In the weak inversion region, the amount of free carriers is sufficiently small in the MOSFET channel to prompt a very small drift current; however, diffusion current still flows through MOS devices (Comer & Comer 2004). In this section, the characteristics of MOSFET in these different inversion regions are analyzed, and their advantage to designers are detailed.

2.3.1. Strong Inversion Region

MOSFETs are most commonly biased in the strong inversion region of operation. In most circuit designs involving MOS devices, discussions are focused on the strong inversion region because their equations are well established. The drain current with respect to the gate-to-source voltage in the strong inversion region is expressed by

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}\,[V_{GS} - V_T]^2[1 + \lambda\,(V_{DS} - V_{DSP})] \tag{2.4}$$

where λ is the channel-length modulation factor, V_T is the threshold voltage, and V_{DSP} is the drain-to-source pinch-off voltage.

2.3.2. Weak Inversion Region

In the weak inversion region, the gate-to-source voltage (V_{GS}) is close to the threshold voltage (V_T), and negligible channel current densities occur. In contrast to the strong inversion whereby the drain current exhibits square law characteristic, in the weak inversion region, the gate-to-source voltage and the drain current relationship can be approximated as

$$I_D = \frac{W}{L} I_{D0} e^{qV_{GS}/nkT} \quad (2.5)$$

where I_{D0} and n may be retrieved from empirical data. The variable n for an NMOS device ranges from 1.3 in the strong inversion region to 1.6 in the weak inversion region (Enz, Krummenacher & Vittoz 1995).

2.3.3. Moderate Inversion Region

The moderate inversion region transitions from weak inversion region to strong inversion region where the diffusion and drift currents are comparable. Moderate inversion is less commonly used because there is no accurate analytical equation for the gate-to-source voltage to the drain current. Figure 4 shows the variation of drain current as a function of effective voltage though which the three inversion regions are illustrated for an NMOS device with a W/L = 100.

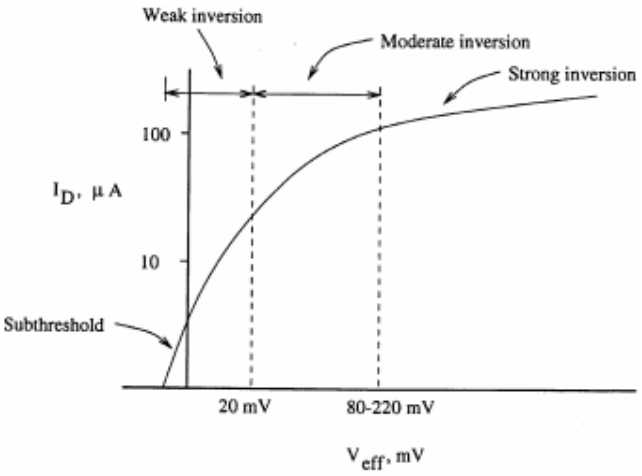

Figure 4: Drain current vs. effective voltage (Comer & Comer 2004).

The biased inversion region of any MOS device depends on the circuit design requirements and its applications. Table 2 shows a comparison between some critical parameters in the three inversion regions.

Table 2: Parameter comparison of the three-inversion region (Lund 2006)

Parameter	Weak Inversion	Moderate Inversion	Strong Inversion
Power consumption	Low	Moderate	High
Transconductance (Gm)	High	Moderate	Low

Transit frequency (F_T)	Low	Moderate	High
VDS(sat)	Min (`~100mV)	130mV – 250mV	> 250mV
Area	Large	Moderate	Small

2.3.4. Short Channel Effects

Substantial development of integrated circuit design has promoted the continuous downscaling of MOS transistors dimensions. Even though the transistor size reduction has economic and technological advantages, it also causes new design challenges such as short channel effects. Currently, with the active device dimension in nanometers, short channel effects may be significant. Short channel effect includes impact ionization, velocity saturation of carrier, drain-induced barrier lowering, and hot carrier injection. Velocity saturation is considered the most crucial short-channel effect causing MOS transistors to deviate from the square law voltage characteristics (Gray 2009). Velocity saturation happens at high electric fields when carrier velocities approach a constant called scattering-limited velocity V_{scl} (Baker & Boyce 2005). Figure 5 illustrates the carrier velocity against the horizontal electric field strength magnitude.

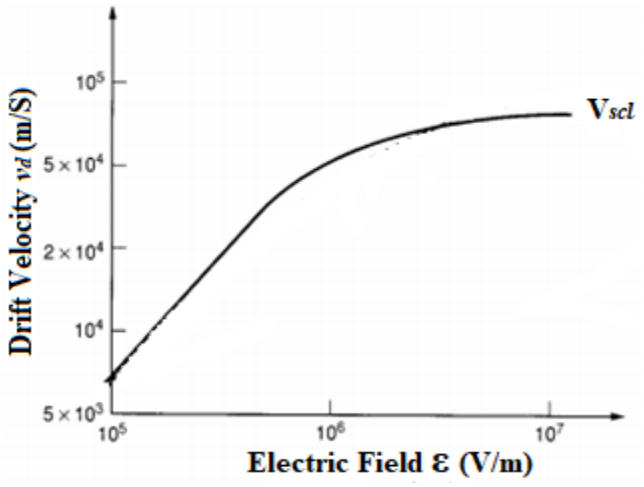

Figure 5: Electron drift velocity against the horizontal electric field in MOS surface channel

The RF power detectors ' circuit configuration in CMOS technology can be established through the understanding of MOSFET's current and voltage characteristics in the different inversion regions. Depending on the design specification, the MOS transistors will be biased in the appropriate inversion region.

2.4. Types of Power detection

Different types of RF power detectors have emerged in recent years to respond to the high demand for precise power detectors. Power detector structure establishes the accuracy of the system. Power detectors can be classified into (i) Peak detection, (ii) Distributed power detectors, (iii) True RMS detection, and (iv) Logarithmic detection. Apart from temperature stability and signal variations with PAR, performance metrics such as operating frequency, area, power consumption, and dynamic range are also crucial in selecting a suitable type of power detector. This section discusses different types of RF power detectors and their impacts on the performance parameters mentioned in the previous section. Each design's advantages and drawbacks are reviewed and discussed to improve our understanding of RF power detector characteristics.

2.4.1. Peak Detection

Peak detectors capture the amplitude of the signal at the input. Two types of peak detectors commonly employed are negative peak detectors that measure the input signal's trough and positive peak detectors that measure the crest of the input signal (Kuphaldt 2011). Peak detection is utilized in constant envelope modulated signal application design such as pulse detection, electronic warfare, envelop tracking in power amplifier, and Global System for Mobile Communications (GSM) (Zhou & Chia 2008). Figure 6 shows a peak detection power detector utilized as an AM demodulator.

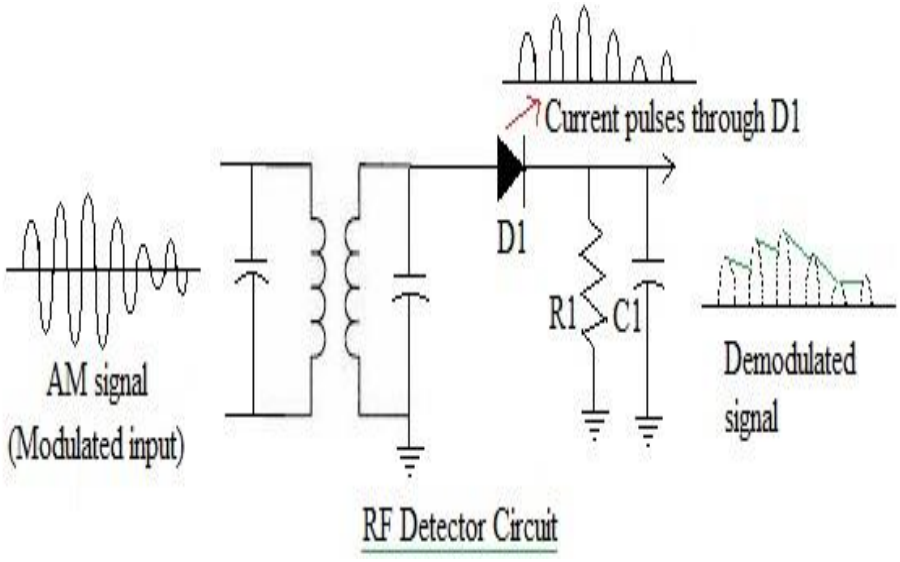

Figure 6: Peak Detector as AM Demodulator (World 2012)

Peak detectors perform power detection by rectifying the input signal with a full or half-wave rectifier. The output signal is then obtained using a low-pass filter (LPF) to average the input signal. In Figure 3, half-wave rectification is achieved by the diode D1 and resistor R1. The capacitor C1 is coupled across resistor R1 to retrieve the original modulated input. The input signal amplitude is proportional to a peak detector's output voltage, and the detected voltage contains the information in the amplitude modulated signal. Peak detection power is commonly accomplished by employing bipolar transistor or diode-based power detectors. However, since bipolar transistors are challenging to implement in CMOS technology, diode-based power detectors are popular for peak detection using CMOS technologies (Zhou & Chia 2008).

Diode-based power detectors were previously extensively used in microwave applications due to their high-frequency characteristics (Milanovic et al. 1996). Diode-based power detectors exploit diodes' nonlinear characteristics to rectify the input signal, generating a DC output proportional to the input amplitude. A simple diode-detector implementation is shown in Figure 7. The diode D1 is an active element that performs power detection. The resistor R1 offers resistive input matching and provides a return path for the rectified current. Resistor R2 acts as the load, and capacitor C1 filters the signal.

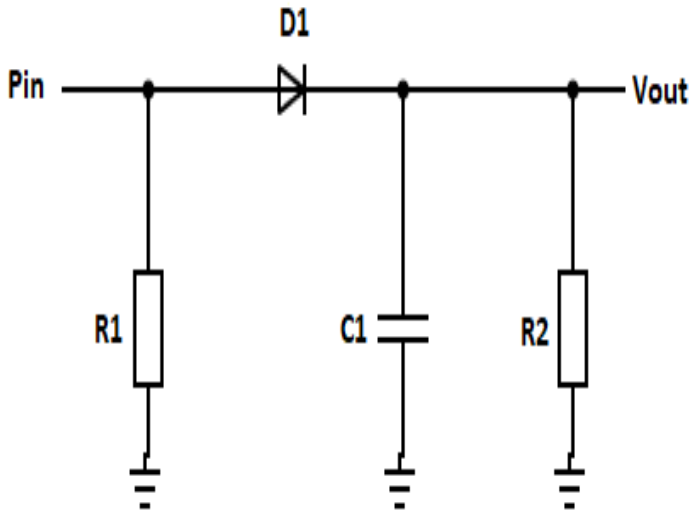

Figure 7: Diode-based power detector

Figure 8 shows the diode I-V characteristic. The I-V characteristic is nonlinear and can be categorized into ‘’linear’’ and ‘’square region’’.

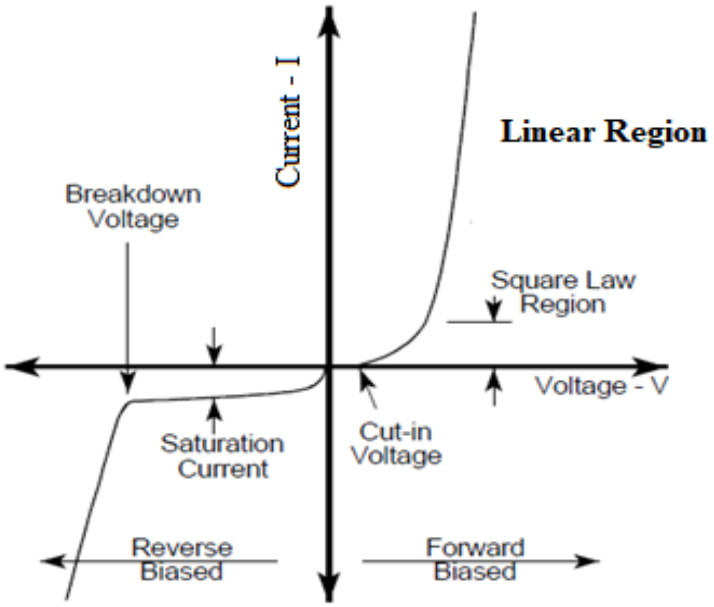

Figure 8: I-V characteristics of a diode (*Detectors*)

In the square region, the detector operates at very small input signal levels, and its output voltage is proportional to the square of the RF input voltage (*Detectors*). This detection region is smaller compared to the linear region. For instance, the square region maintains noise levels at around -20 dBm in a standard commercial diode, and the linear region extends above 0 dBm. Consequently, diode-based power detectors have a limited dynamic range of about 18-25 dB. The linear region is functional for larger signal levels. In the linear region, the input signal envelope changes linearly with the output signal (*Detectors*). Figure 9 illustrates a more practical diode model, which includes a parasitic capacitance C_P and an internal series resistance Rs.

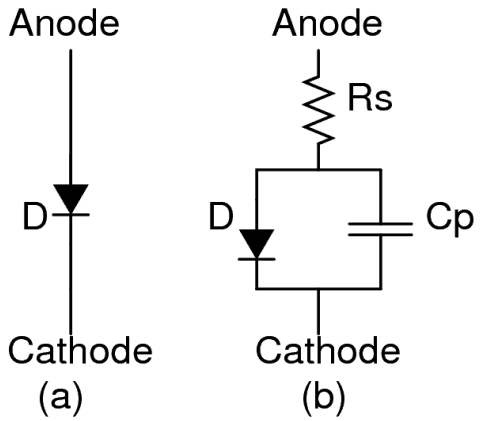

Figure 9: The (a) Ideal diode (b) a more practical diode

The diode's small-signal resistance is very small for larger signals. As such, the internal resistance Rs begins to dominate for larger signals, as illustrated in Figure 9. Therefore, the internal resistance Rs, V/I, will then limit the current resulting in a linear signal. Diode-based detectors offer the fastest response time constant compared to the other design implementations (Thanachayanont 2015). Fast response time is a vital specification for applications involving wireless communications.

Nonetheless, since the diode junction is temperature dependent, the output rectified voltage changes with temperature (Fei 2007). Besides, limited dynamic range, the temperature dependency of the diode junction is another significant limitation. However, the temperature dependency can be reduced by implementing a resistor and a second identical diode, as shown in Figure 10.

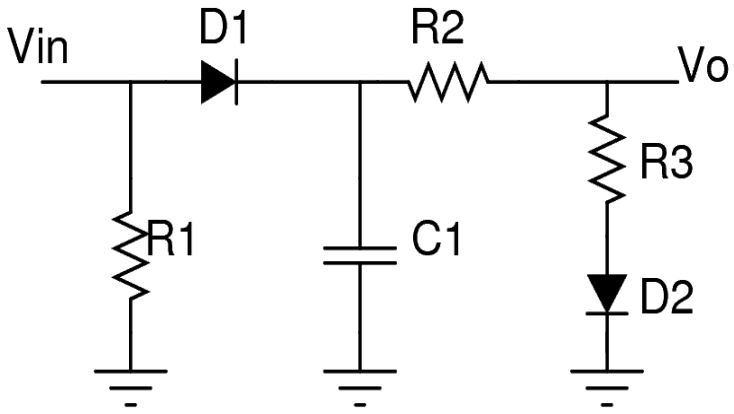

Figure 10: Temperature-compensated diode-based power detector

From Figure 10, assuming that R2 and R3 are identical and currents into and out of node Vo are the same, we can write

$$\frac{V_{R1}}{R2} = \frac{V_{R3}}{R3} \rightarrow \frac{\hat{V}_{in} - V_{D1} - V_{OUT}}{R2} = \frac{V_{OUT} - V_{D2}}{R3} \tag{2.6}$$

Since R2 and R3 are identical, the equation simplifies to

$$\hat{V}_{in} - V_{D1} - V_{OUT} = V_{OUT} - V_{D2} \tag{2.7}$$

Since V_{D1} and V_{D2} are identical and then solving for Vo leads to

$$V_{OUT} = \frac{\hat{V}_{in}}{2} \tag{2.8}$$

Equation (2.8) demonstrates that the detector's temperature dependence is eliminated with the addition of a second identical diode. Equation (2.8) also proves that a diode-based detector measures the peak power, which varies with PAR's. Furthermore, it is important to note that the cost of large chip area, power consumption, and matching circuits of diode-based detectors are significant design considerations for applications in the gigahertz region.

In a recent paper (Li et al. 2019), a diode-based power detector was developed in a 65 nm CMOS process to improve the maximum input power and dynamic range through a balanced switched capacitor architecture for wireless microwave power transfer (MPT) applications. Their power detector consisted of four PN junction diodes operating as switches, an output filter for high frequency, a load resistor, and two capacitors at the input. The diode's bias voltage is below the threshold voltage, which resulted in low power consumption of 0.7 mW. The diodes operated as power detectors both in the negative half-cycle and positive half-cycle to enhance linearity, thus the dynamic range. In another paper, Milanovic (Milanovic et al. 1996) developed a Schottky diode power detector using a 2 μm n-well CMOS process on both n-well and p-substrate. The diode detector circuit consisted of a 75-pF surface-mount capacitor, a Schottky diode on a CMOS chip, and a 51 Ω surface-mount matching resistor. The dynamic range and operating frequency obtained through a simple half-wave detector circuit were 50 dBm and 50 MHz to 20 GHz. However, the high parasitic capacitance of the device made it unsuitable for high-frequency applications.

Comparatively, commercially available diode-based power detectors can offer up to a 90 dB dynamic range. A range of -70 dBm to 20 dBm is available for single-path models optimized for continuous-wave measurements (Brush 2007). For instance, ON Semiconductor fabricated an NCS5000 power detector with an integrated Schottky diode for communication systems applications. The power detector has a simple configuration for operation up to 2 GHz and a dynamic range of 50 dBm. The power detector can operate at a low supply current of 300 μA for a temperature range of -40 °C to 85 °C (Semiconductor 2006). The higher dynamic range of commercially available diode-based power detectors is due to the high speed SiGe fabrication process.

2.4.2. True RMS Detection

True RMS power detector, also referred to as RMS-to-DC converters, is a popular design methodology due to their insensitivity to Peak-to-Average envelope power Ratio (PAR) compared to peak and logarithmic detection. These power detectors generate a quasi-DC signal representing the power level of an input signal. The different types of RMS detectors implementation are described in this sub-section.

Thermal Detection

In theory, thermal detection is one of the simplest RMS power detector methods; however, it is difficult and expensive to realize (Akin 2005). Thermal detection is commonly used in communication and sensor applications due to its high accuracy and wide bandwidth (Erikson & Waugh June 2000). Figure 11 shows an RMS power detector implemented with thermal detection. Both the reference voltage and the input signal heat the adjacent thermocouples and a resistor individually. The temperature is proportional to the induced output voltage. The difference between these output voltages is a scaled measure of the input power relative to the reference power.

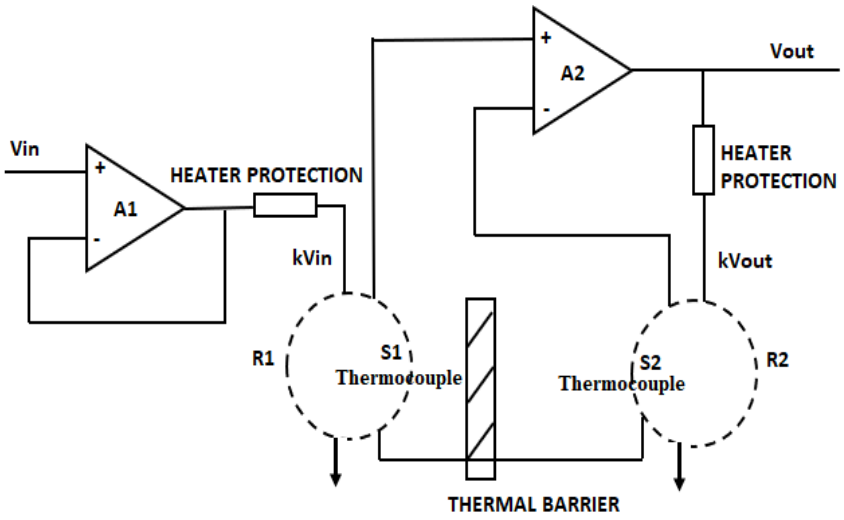

Figure 11: Implementation of a power detector with thermal detection (Cowles 2004)

Thermal isolation and matching among the thermocouples to reduce dependency are crucial for better accuracy. This implementation has excellent accuracy as the power is proportional to the temperature differences (Brush 2007). However, this system is challenging to integrate and implement in standard CMOS and has high power consumption. Temperature gradients produced

by adjoining circuits can also lead to operation failure. Moreover, slow thermal-time constants can limit the response time of such systems (Cowles 2004).

Power Detector Using a Single FET

Field-effect transistors (FETs) have higher ease of integration with different technology processes in comparison to diode-based or thermal-based power detectors (Ferrari et al. 2005; Piovani & de Sousa 2011). Furthermore, FETs offer better sensitivity to temperature variations as compared to Schottky diodes. A power detector implemented using a single NMOS is presented in Figure 12. The square-law characteristic of the NMOS transistor M1 is exploited to perform power detection. The transistor is biased in the saturation region, and the input signal is applied through the drain of the device. Resistor R3 acts as a load to establish the output voltage while C3 and R2 filter the output signal.

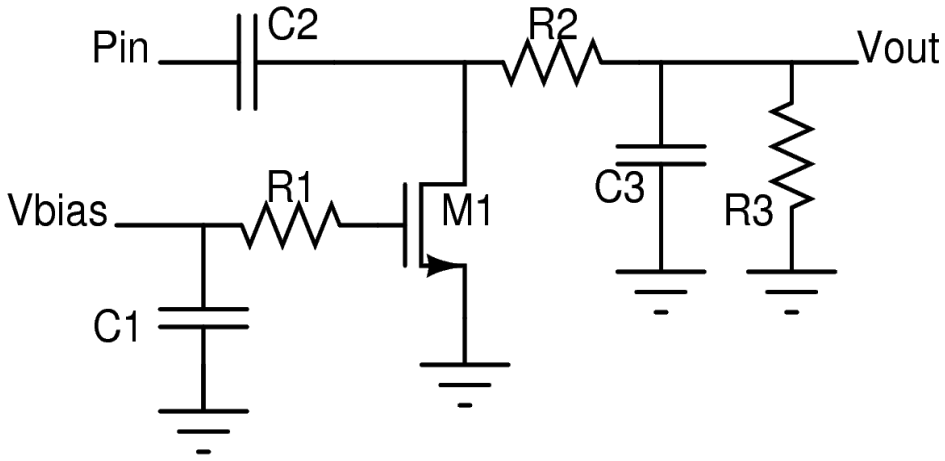

Figure 12: Power detector with single FET

In literature, Ratni et al. (Ratni et al. 1998) fabricated a power detector using a single FET in silicon with MOS technology to overcome sensitivity to temperature variations exhibited by Schottky diode. A common gate structure was used along with optimum biasing close to the borderline between the saturation and triode region. In the saturation region, the equation relating the drain current and gate-to-source voltage neglecting channel length modulation is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (2.9)$$

where W and L are the transistor's physical dimensions, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, C_{ox} and μ_n are the capacitance per unit area, and the average electron

mobility, respectively. The square-law of the active device was exploited to realize power detection (Ratni et al. 1998). The measured results show a dynamic range of around 20 dB for a frequency range of 1 GHz to 2 GHz.

Differential Structure

A single-ended power detector's performances suffer from process and temperature variations, which affect the output of the power detector (Fei 2007). A differential structure would alleviate this issue. Generally, differential power detectors have one active device connected to the microwave power input and another similar active device, which acts as a reference point. The second device will reduce the DC voltage offset caused by the supply voltage and temperature variations (Thanachayanont 2015). Moreover, the differential signal has higher immunity to common-mode noise when compared with a single-ended device (Xu et al. 2014). Figure 13 shows a differential microwave power detector employed by (Zhou & Chia 2008). This power detector was designed using 0.13 μm CMOS technology which exploited the square-law characteristic of MOS transistors in the strong inversion region to detect microwave signals. The two transistors M1 and M2, are identical and biased through the same condition. The RF signal is applied to NMOS M1. The drain current of the two transistors was given by

$$I_1 = \frac{K}{2}\frac{W}{L}(V_{GS} + V_{rf} - V_{TH})^2 \quad (2.10)$$

$$I_2 = \frac{K}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (2.11)$$

$$K = \mu_n C_{ox} \quad (2.12)$$

Where V_{GS} is the biasing voltage, L and W are the length and width of the transistor, respectively. V_{TH} denotes the threshold voltage, C_{ox} and μ_n, the capacitance per unit area, and the average electron mobility. Assuming that the input signal $V_{rf} = V_i\cos(\omega t)$, thus

$$I_1 - I_2 = \frac{K}{2}\frac{W}{L}{V_{rf}}^2 + \frac{KW}{L}V_{rf}(V_{GS} - V_{TH}) \quad (2.13)$$

$$= \frac{K}{4}\frac{W}{L}{V_i}^2 + \frac{K}{4}\frac{W}{L}{V_i}^2\, cos(2\omega t) + \frac{KW}{L}(V_{GS} - V_{TH})V_i\cos(\omega t) \quad (2.14)$$

Then differential output voltage, which is proportional to the input power, is given by

$$V_o = \frac{K}{4}\frac{W}{L}RloadV_i^2 \quad (2.15)$$

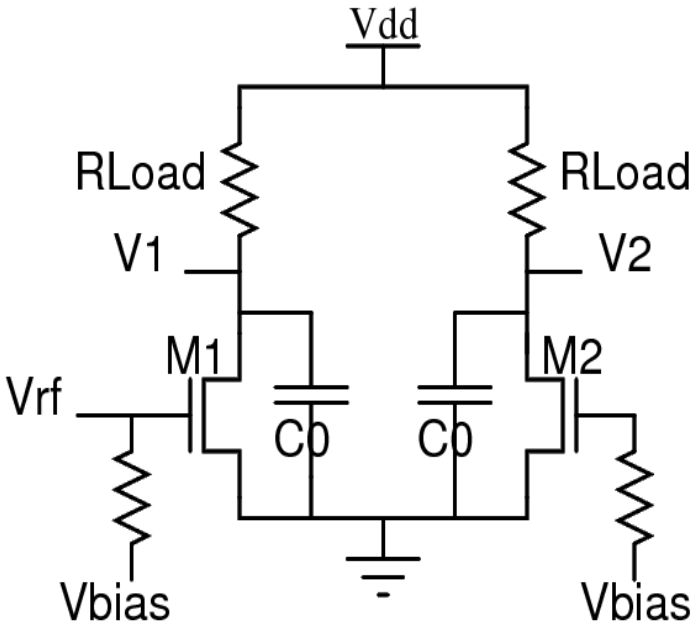

Figure 13: A power detector based on the differential structure (Zhou & Chia 2008)

Their proposed design also consisted of an exponential current generator, a differential power detector unit, and a two-stage operational amplifier. Linear-in-decibel output was obtained by biasing the exponential generator's transistors in the weak inversion region so that its drain current (I_{DS}) is the exponential of the gate to source voltage (V_{GS}). The operating frequency was from low frequency to 8.5 GHz, and the static power consumption was 0.18 mW. However, though a low power consumption was achieved, the exponential generator transistor limited the highest detectable signal levels resulting in a lower dynamic range. Furthermore, since the MOSFETs operating in the weak inversion region are temperature dependent, the author (Zhou & Chia 2008) suggested that a temperature and process compensation circuit should be included for better accuracy.

Squaring Cell Detection

Another design strategy for RMS power detectors is squaring cells (SQRs). Squaring cells consist of nonlinear elements such as MOSFETs generating an output voltage proportional to the input voltage's square. These squaring cells perform squaring and averaging to obtain the RMS voltage of the input signal. The output of the squaring cells contains power information. Squaring cells are categorized as explicit RMS power detectors as a result of their straightforward squaring, averaging, and square rooting (Counts. 1986; Kafe & Psychalinos

2014). These Squaring cells are classified into three modes: current-mode, voltage-mode, and voltage/current-mode (Al-Absi & As-Sabban 2014). Furthermore, they can be designed using different methodologies such as Meyer squaring structure and MOSFETs Translinear Loop (MTL) (Tao, Eisenstadt & Fox 2004). Choi (Choi et al. 2016) developed a wide dynamic range RMS power detector using a 28 nm CMOS standard process. Their proposed power detector consisted of a trans-impedance amplifier (TIA), cascading gain amplifiers (GAs), differential to single-ended amplifier (D2S), and squaring circuits (SQRs). A power level segmented detection approach was employed to realize more than 40 dB dynamic range. The RF input is first applied to the GAs and converted to a squared DC voltage by the squaring cells for averaging. Figure 14 shows their proposed design.

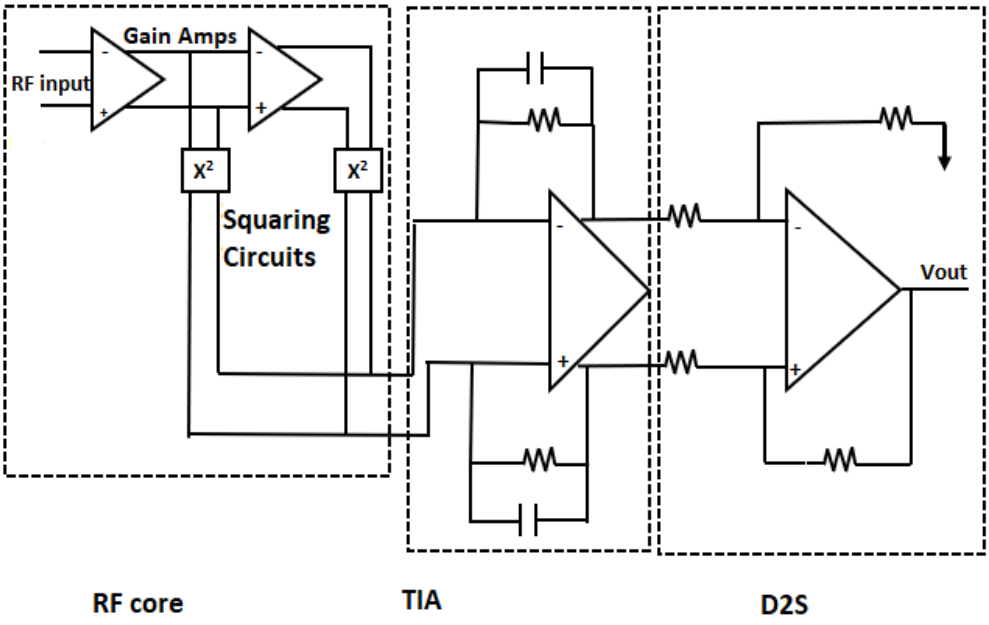

Figure 14: Microwave power detector using squaring cells (Choi et al. 2016)

The transimpedance amplifier converted the output current from the GAs and squaring cells block to voltage with the help of a feedback resistor. Finally, single-ended voltage is realized using the D2S. The dynamic range could be extended if required by using more GAs and squaring cells. The Meyer squaring architecture was utilized to repress odd harmonics terms and common mode variations. DC offset calibration is required due to mismatches in the circuit, which considerably affects the squaring cell's dynamic range. The power detector's operating frequency was from 0.7 GHz to 4 GHz with a dynamic range greater than 40 dB and power

consumption of 5.8 mW. Squaring cells' insensitivity to modulation form or signal shape due to averaging over time makes them suitable for cellular RF integrated circuits (RFICs) applications. One limitation of squaring cells implemented in CMOS technology is mismatches that reduce the detection range considerably.

Rectifier Implementation

Rectifier microwave power detectors are uncommon due to their high power consumption. However, they do have applications in on-chip RF measurement. An unbalanced source coupled pair is usually used to design current amplifiers (Nash 1999).

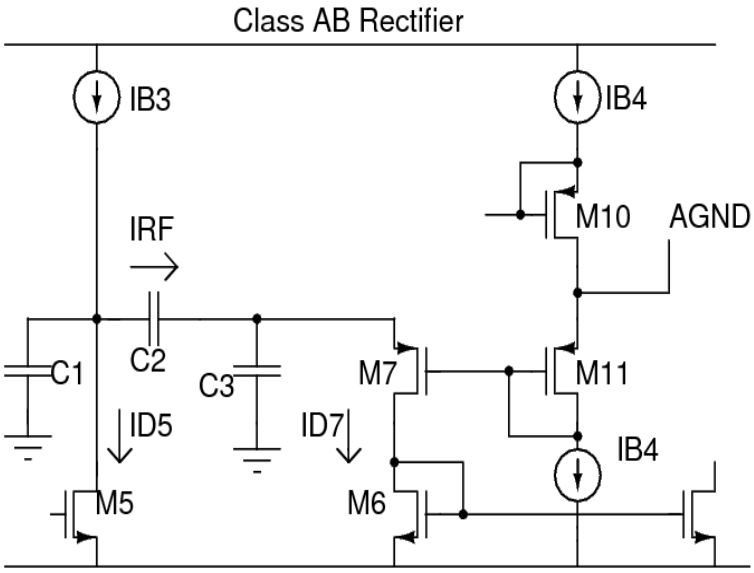

Figure 15: Schematics of the rectifier with parasitics employed in (Valdes-Garcia et al. 2008)

Valdes-Garcia et al. (Valdes-Garcia et al. 2008) employed a class AB rectifier demonstrated in Figure 12 to implement an RF power detector using a 350 nm standard CMOS process. The input voltage was converted into current and amplified by a high input impedance input stage. The circuit operated in current mode, and the rectifier then performed full-wave rectification of the current at the first stage. The class AB rectifier rectifies the current only if the operation is in the nonlinear region. The circuit also consisted of an LPF to extract the DC components. The power detector had an operating frequency range from 0.9 GHz to 2.4 GHz, a conversion gain of 50 mV/dBm, a dynamic range greater than 30 dB, and power consumption of 8.6 mW, including the bias circuits.

Log-Antilog Detection

Log-Antilog detection is also a less popular design employing nonlinear circuit components in which the output voltage is proportional to the exponent (logarithm) of the input. Log-Antilog circuit can perform processes such as division and multiplication using subtraction and addition of logs. Log-Antilog circuits use the exponential relationship of a junction to implement other functions such as

$$ln(x^n) = nln(x) \tag{2.16}$$

to perform RMS power detection. Given equation (2.19), the square-root and square function can be expressed as

$$ln(x^{0.5}) = 0.5ln(x) \tag{2.17}$$

$$ln(x^2) = 2\ln(x) \tag{2.18}$$

Figure 16 shows a block diagram representing the log-antilog RMS detection. It is important to note that the input current (i_{IN}) is assumed to be always positive.

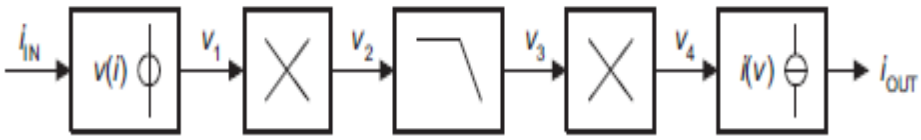

Figure 16: Log-Antilog detection block diagram (Petrofsky 2002)

The input current is first applied to a forward-biased semiconductor junction which generates a voltage proportional to the input current natural logarithm (exponent). A multiplier circuit then doubles this voltage and generates the input current square function.

$$v_1 = \ln(i_{IN}) \tag{2.19}$$

$$v_2 = 2\ln(i_{IN})$$

$$= ln\left(i_{IN}{}^2\right) \tag{2.20}$$

A low-pass filter (LPF) then averages and filter the voltage.

$$v_3 = \overline{ln(i_{IN}{}^2)}$$

$$\approx \ln\left(\overline{i_{IN}{}^2}\right) \qquad for\ i_{IN} > 0 \qquad (2.21)$$

The average voltage is then halved using a divider circuit to generate the averaged, squared input current square-root function.

$$v_4 = \frac{1}{2} ln\left(\overline{i_{IN}{}^2}\right)$$

$$= ln\left(\sqrt{\overline{i_{IN}{}^2}}\right) \qquad (2.22)$$

Subsequently, the halved voltage is applied to another forward-biased semiconductor junction generating an output current proportional to the input current RMS value.

$$i_{OUT} = e^{ln\left(\sqrt{\overline{i_{IN}{}^2}}\right)}$$

$$= \sqrt{\overline{i_{IN}{}^2}} \qquad (2.23)$$

Very low power consumption and chip area are the main advantages of log-antilog RMS detection. However, log-antilog RMS detection also has various limitations making them a less popular design implementation for RF power detector design (Petrofsky 2002). One of the main disadvantages is that the input current must be continuously positive for all logarithmic computations. In the case of negative input current, an absolute value circuit must precede the log-antilog RMS detector. Absolute value circuits are difficult to implement and integrate with CMOS technology due to amplitude-dependent errors, polarity gain mismatch, and offset errors. In addition, since log-antilog detectors are sensitive to noise and mismatch, the dynamic range is limited (Aa 2006; Bitzer, Schmidt & Simmer 2006). Furthermore, the typical signal levels are greater than the signal's amplitude between the two forward-biased semiconductor junctions. This condition can worsen mechanical stress, thermal drift, and component tolerances (Petrović 2015; Skinner & Lambert 2009).

2.4.3. Distributed Power Detectors

Distributed Power detectors are a design that solves the issues of wideband input matching arising from established matching methods such as reactive and resistive matching (Qayyum & Negra 2018). The principle of operation of such power detectors relies on the diode’s parasitic junction capacitance coupled with a lumped inductive element to perform RF power detection

(Shillady 1986). Distributed power detectors achieved higher bandwidth through absorption of the diode's parasitic junction capacitance in a traveling-wave structure. As such, input power dissipation through matching resistors is prevented, leading to higher voltage sensitivity, suitable for communications receiver applications.(Qayyum & Negra 2018).

In a recent review, Qayyum & Negra (Qayyum & Negra 2017b) developed a distributed power detector using a 130 nm CMOS technology in a traveling-wave structure. The transconductance of the transistors for power detection was biased in the weak inversion region to enhance the voltage sensitivity. Figure 17 shows the schematic of the power detector proposed by Qayyum & Negra. The power detector comprises three MOSFETs biased in the subthreshold region, a coupling capacitor ($C_{coupling}$) at the input, a DC blocking capacitor (C_{block}), resistors, and inductors. The proposed power detector transmission line impedance Z_{line} determines the impedance input matching. Z_{line} is expressed by $\sqrt{(L_{line} / C_{in})}$ where C_{in} is the power detector stage input capacitance. The transmission line is terminated by an on-chip DC blocking capacitor and a 50 Ω resistor.

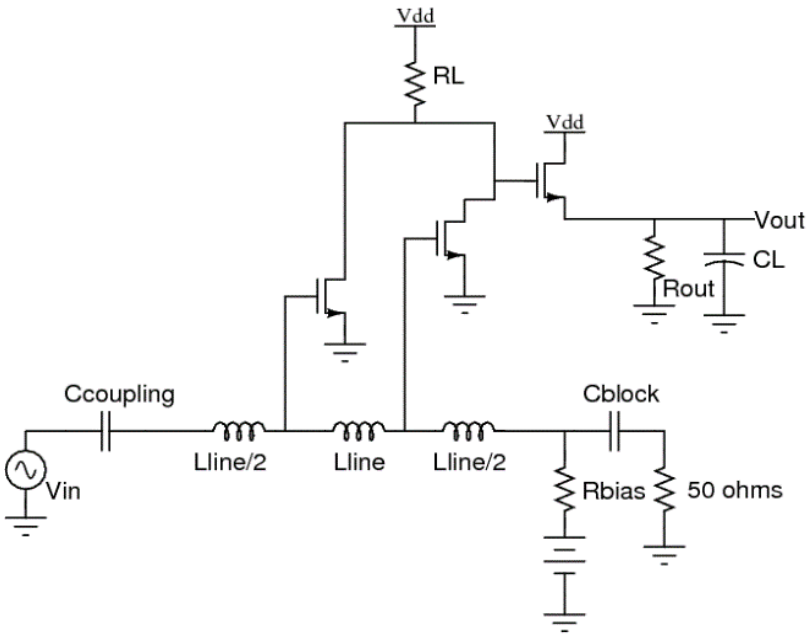

Figure 17: Schematic of distributed power detector employed in (Qayyum & Negra 2017b)

The power detector operated from 7 GHz to 70 GHz with an overall voltage sensitivity of 75 dB and power consumption of around 0.156 mW. Qayyum & Negra demonstrated that the minimum detectable input power is within -40 dBm and -37 dBm. However, this design is more suited for

high voltage sensitivity microwave applications such as radiometers and communication receivers. Other performance metrics of the power detector were not discussed in detail (Qayyum & Negra 2017b).

2.4.4. Logarithmic Detection

A high dynamic range is an essential requirement in the design of most RF power detectors. A dynamic range of 50 dB and above is generally realized by logarithmic detectors. Log-amp limiters are a popular and efficient design strategy to extend the dynamic range. Figure 18 presents the transfer function of a logarithmic power detector. As shown in Figure 18, the logarithmic power detector's RF input power varies linearly with the output voltage. Linear in-decibel characteristics are important in wireless communications applications because, as mentioned in previous sections, power levels are typically specified in dBm.

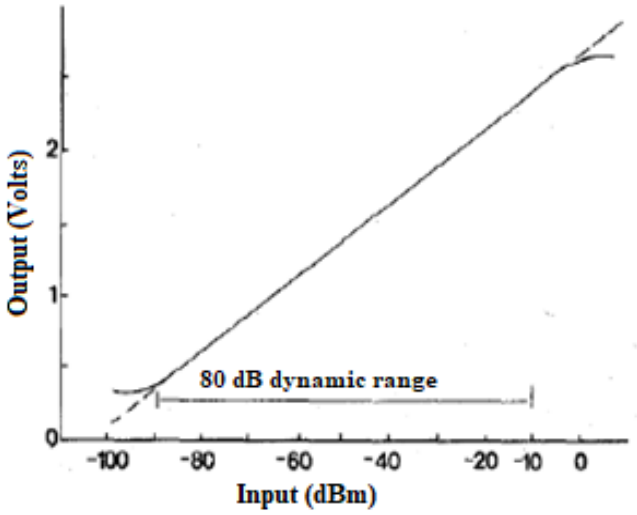

Figure 18: Logarithmic power detector transfer function (Barber & Brown 1980)

The logarithmic power detector's main objective is to compress wide dynamic range signals into the decibel equivalent. When the logarithmic power detector transfer function is appropriately calibrated, it can be used as a precise measurement device that expresses input signal AC amplitude in the logarithmic domain. Furthermore, one significant edge of the logarithmic detector is its ability to represent large input voltage variations by relatively small changes in the logarithmic power detector output voltages. To realize wide dynamic range, logarithmic power detectors utilize combined output from low gain limiting amplifiers to approximate the logarithmic power detector's input-output characteristics. The logarithmic detector usually uses a

piecewise linear approximation to achieve linear-in-decibel output through progressive compression of the input signal. Figure 19 shows the architecture of a logarithmic power detector.

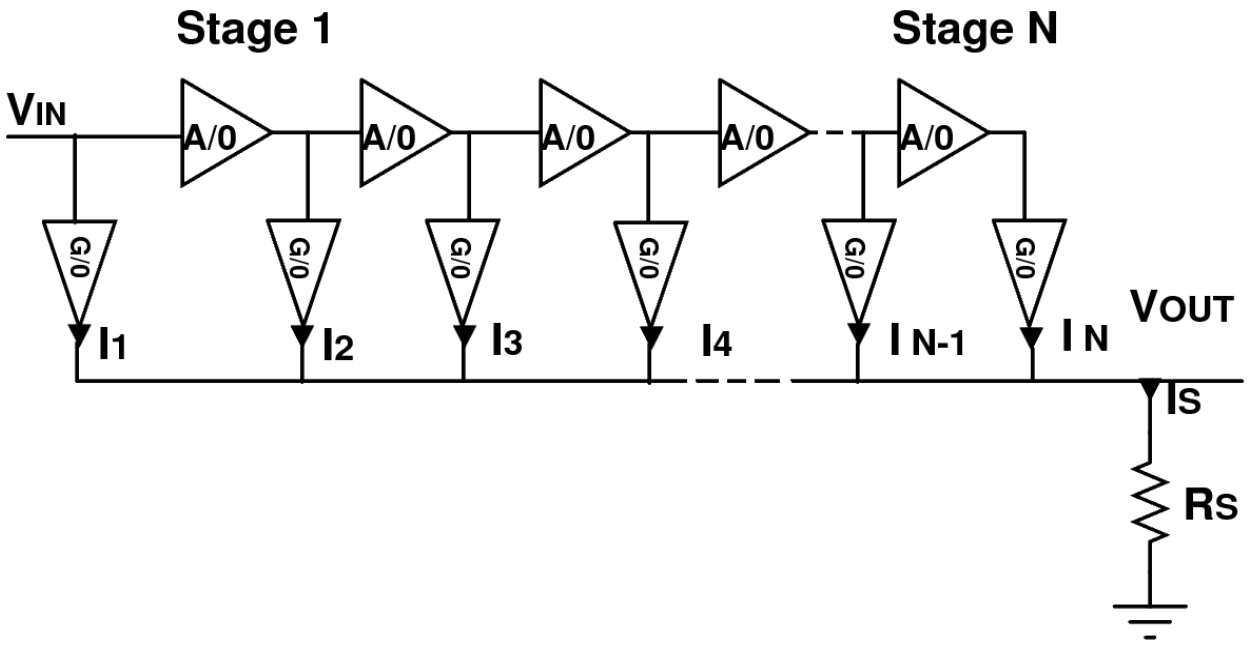

Figure 19: Architecture of a logarithmic power detector (Muijs 2013)

When the input signal amplitude V_{IN} is increased, each gain stage begins compression. The limiter provides gain and clips the output at a specific voltage level. The limiter closest to the output will reach the maximum level first and then progress towards the input. The limiter is then connected to the G/0 stages that produce output currents proportional to the signal voltages at these specific points. The output currents are summed and applied to a resistor to generate the linear-in-decibel output (Thanachayanont 2015). Usually, the configuration shown in Figure 19 will only operate for quasi DC input voltage. A typical logarithmic power detector should convert an AC signal to a pulsed DC output voltage. As such, the G/0 stage is modified to perform rectification function. The rectified voltage is then filtered using a low-pass filter to remove the ripples.

The limiter is usually designed with low gain and high bandwidth for better accuracy and operation at high frequencies and under small-signal conditions. The logarithmic detector has a relatively fast response time and excellent temperature stability. Furthermore, a higher number of

cascaded gain stages will increase linear-in-decibel performance. However, the power consumption increases with an increasing number of stages, so design tradeoffs are required.

In recent literature, Chou et al. (Chou et al. 2017) developed a logarithmic power detector using 90 nm CMOS technology; however, millimeter-wave amplifiers were employed instead of limiting amplifiers for the gain cells. Millimeter-wave amplifiers were proposed to solve the limited bandwidth problem of the limiting amplifiers, thus enhancing the dynamic range. The circuit consisted of three millimeter-wave amplifiers and four rectifiers. Single-ended common-source architecture operating in the saturation region was used to design the rectifiers. The proposed design measurement results displayed low power consumption, high dynamic range, and acceptable log errors.

In an attempt to improve the low dynamic range in (Zhou & Chia 2008), a power detector with a current mirror active load and a logarithmic amplifier was designed by (Sakphrom & Thanachayanont 2012). The microwave power detector's architecture consisted of a differential power detector unit, a seven-stage logarithmic amplifier, a supply voltage, a process, and a temperature-insensitive current reference circuit for optimum biasing. The RF input signal was applied to the differential power detector unit and converted into a DC output voltage which was further amplified by the seven-stage logarithmic amplifier. Figure 20 shows the RF logarithmic power detector employed in (Sakphrom & Thanachayanont 2012).

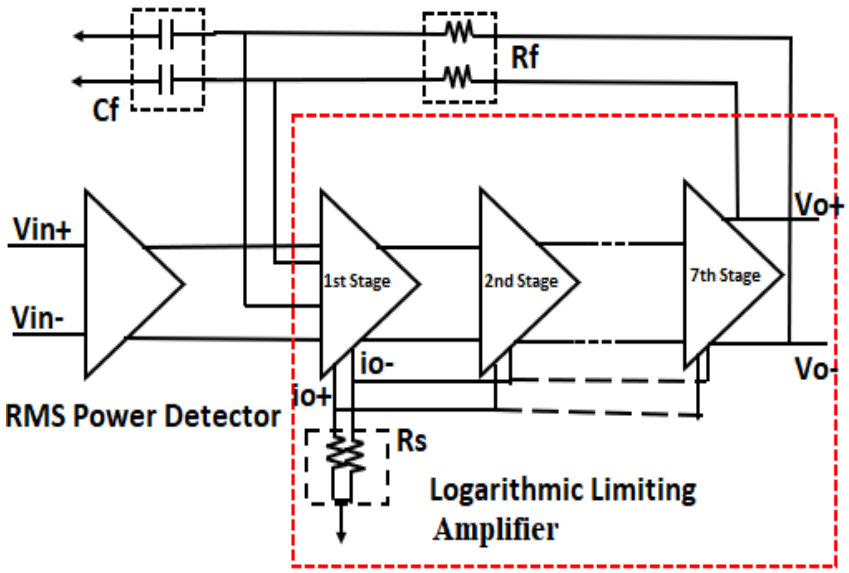

Figure 20: Log-amp limiter power detector (Sakphrom & Thanachayanont 2012)

Linear-in-decibel output was realized using a piecewise linear approximation. Since the power detector's input was DC voltage, rectifier, and filters were omitted from the logarithmic amplifier circuit design, resulting in comparatively lower power consumption (Sakphrom & Thanachayanont 2012). A high output resistance was set to achieve a higher conversion gain, considerably improving the power detector's sensitivity and linearity.

2.5. Applications

Several applications involving power detectors to monitor signal levels in wireless communication were mentioned in the previous section. This section will discuss some of those applications and introduce other applications of RF power detectors.

2.5.1. Power Gain Calculation

Logarithmic power detectors are commonly employed for power gain calculation. Theoretically, the power gain is determined from the division of output power level from the input power level (Nash 1999). Since division is a complicated math operation in an analogue circuit, a logarithmic RF power detector is employed to simplify the circuit implementation. When both power levels are logarithmic quantities, the system's power gain is obtained from the input power's subtraction from the output power. Figure 21 shows an example of a power gain calculation circuit implementation.

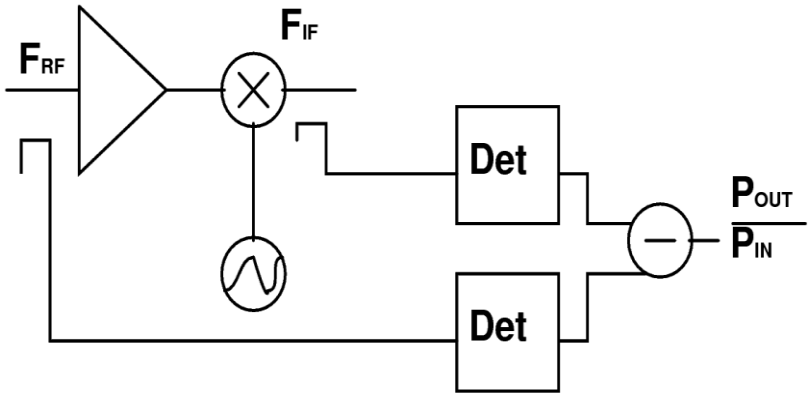

Figure 21: Power gain calculation circuit (Bleeker 2012)

The system consists of one directional coupler that generates a signal proportional to the Intermediate Frequency (IF) output signal and a second coupler that produces an output signal proportional to the RF input signal. The output signal generated from both logarithmic power detectors is then subtracted from one another to determine the power gain.

2.5.2. Voltage Standing-Wave Ratio (VSWR) measurement

Voltage Standing-Wave Ratio (VSWR), often associated with radio technology, is the peak voltage ratio along a transmission line to minimum voltage (Microwaves101 2021).

$$\Gamma = \frac{V_{Reflected}}{V_{Forward}} \tag{2.24}$$

where ɾ is the reflection coefficient. Figure 22 shows the configuration of a simple VSWR measurement system. The maximum power transfer occurs when both the transmitting and receiving end impedances are equal (Rizk et al. 2016). Nevertheless, it is challenging to achieve in a wireless system due to variations of the antenna's surroundings. When the antenna's surroundings change, there can be severe effects on the input port impedances resulting in minimum power transfer, thus a large VSWR (Nielsen et al. 2005). Large VSWR may lead to several problems, such as damaged transmission lines and power amplifiers. In a communication system, the protection of transmission lines and power amplifiers is crucial. As such, VSWR measurements are utilized to measure impedances mismatch and avoid these problems.

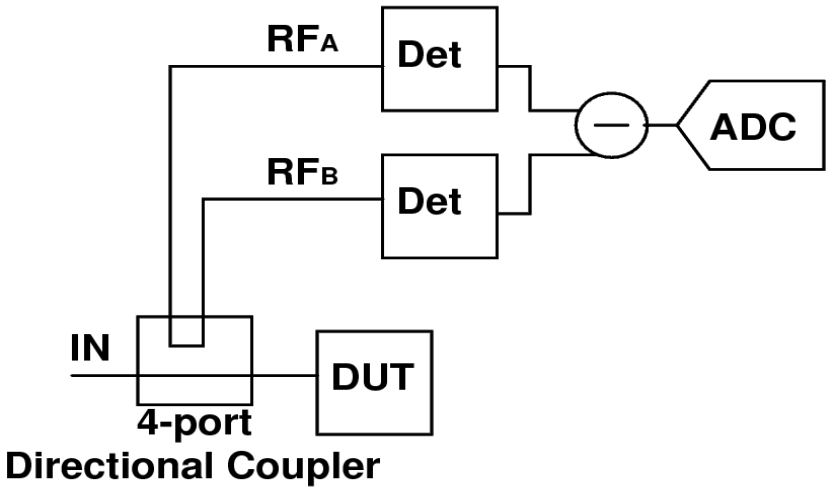

Figure 22: VSWR Simplified Measurement System (Nielsen et al. 2005)

As shown in Figure 22, the VSWR measurement system consists of one directional coupler utilized to separate the transmission lines reflected and forward power waves between the antenna and the power amplifier. Additionally, a secondary output of the directional coupler produces a signal proportional to the reflected power waves, while the other secondary output produces a signal proportional to the forward power waves (Bleeker 2012). The output signals generated from both logarithmic power detectors are then subtracted from one another.

2.5.3. Modern Wireless Transmitters Power Measurement

The transmitted RF power in modern wireless transmitters usually demands strict control so that the cell size of wireless cellular networks can be set accurately to improve coverage. In addition, precise measurement in the power control loop makes the RF power amplifier thermal dimensioning easier for conditions where uncertainty about the actual transmitted power resides. As such, a 47 dBm (50 W) power amplifier with an uncertainty of 1 dB must be dimensioned safely so it can transmit 48 dBm (63 W) without overheating in the control loop (Aa 2006; Nash). RMS detectors are usually preferred for precise measurement of signals in wireless cellular networks due to the variations of signal peak-to-average ratio. Figure 23 shows a simplifier block diagram of an RF power detector used as a precise measurement device in a modern wireless transmitter.

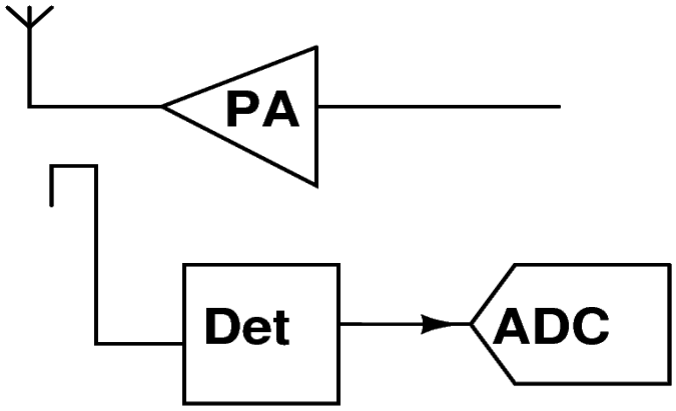

Figure 23: Simplified block diagram of an RF power detector employed in a modern wireless transmitter (Bi et al. 2019)

The RF power detector, when employed as a measurement device in modern wireless transmitters, operates as follows:

Such a measurement system comprises an RF power detector, a directional coupler, a power amplifier, and analogue to digital components. First, part of the power amplifier energy from the output voltage of the RF power detector is collected using the directional coupler with minimum impact on the original RF input signal. Then the analogue to digital converter digitizes the detected RF power. Finally, given the digitized RF power measurement, a decision is established upon the measured output power vs. desired output power. Besides the configuration shown in Figure 23, alternative approaches such as the dynamic control loop can be employed in a

feedback control circuit to precisely control the transmitted power. The benefit of such configuration is that despite variations in temperature, voltage, and environmental conditions, the PA can still maintain the bias condition for performance optimization (Shieh et al. 2009). In short, with the addition of feedback control, the transfer function of the power amplifier is eliminated from the overall transfer function (Bleeker 2012; Raab et al. 2002).

2.5.4. Receiver end Input Measurement

Power measurement at the receiver end, called the received signal strength indicator (RSSI), is utilized with automatic level control (ALC) or Automatic Gain Control (AGC) to control the receiver channel gain, thus maintaining a stable signal level. Figure 24 shows a power detector employed with an ACG loop to have a consistent signal at the Analog to Digital Converter (ADC).

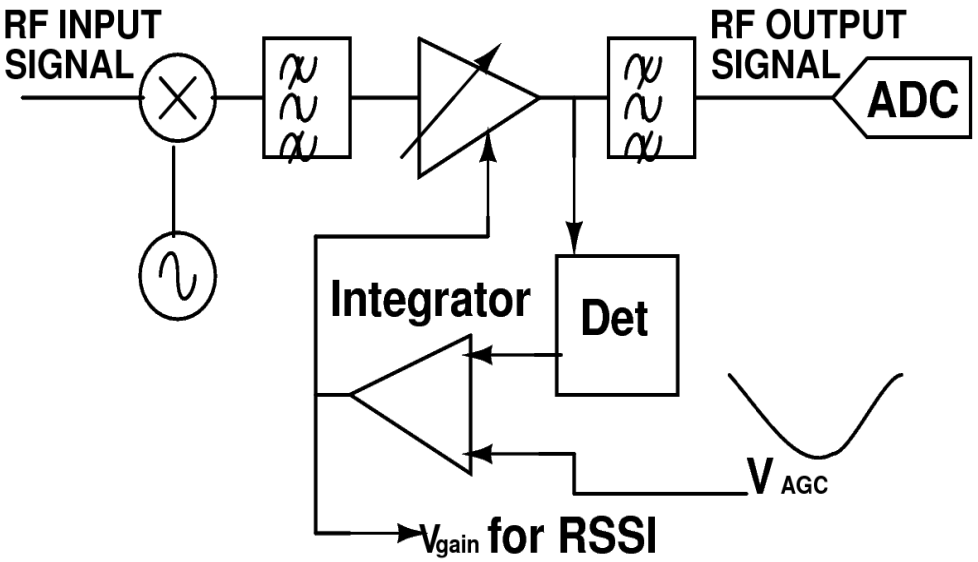

Figure 24: Power detector employed with AGC at the receiver end (Moody et al. 2019).

These systems usually require a higher dynamic range of around 80 dB. Environmental conditions can cause variations of signal power levels at the receiver end over a wide dynamic range (Holdenried et al. 2002). In addition to that, when the input signal is very small, it will waste useful dynamic range, while when it is very large, the ADC input will overdrive (Helhel, Göksu & Ozen 2008). Consequently, it is crucial to maintain a consistent signal power level using the ADC's whole dynamic to obtain a high signal-to-noise ratio (SNR). RF power detectors together with an AGC loop are employed to provide signal levelling in receivers.

2.6. Critical Review

This study focuses on implementing a low-power microwave power detector with a linear-in-decibel output for various wireless communication systems applications. In prior sections, we have depicted the different types of power detectors. Form the analysis and discussion; presently, we clearly understand each power detector's advantages and limitations. Table 3 presents an outline of these differences.

Table 3: Comparison of the different implementation strategies

Design Methodologies	**Advantages**	**Drawbacks**
Peak detection	• Simpler Circuits • Fast Response	• Output voltage varies with PAR • Limited dynamic range • Inaccuracy at high frequencies • Poor temperature stability
Logarithmic detection	• Wide dynamic range • Linear-in-decibel output • Excellent stability and accuracy • Fast Response	• High Power Consumption • Output voltage varies with PAR
Distributed Power detectors	• Better wideband input matching • Higher sensitivity • Lower NEP	• Limited dynamic range • No linear-in-decibel output
True RMS Power detectors	• Output voltage does not vary with PAR • Good Stability	• Limited dynamic range • Slow Response Time

Table 4 summarizes a list of different design methodologies found in literature. Their operating parameters and applications are also presented. Table 4 shows that log-amp power detectors provide a higher dynamic range of up to 50 dB compared to the other design methodologies. Due to the progressive compression and the cascaded low gain limiting amplifiers, their high dynamic range makes the log-amp limiter suitable for GSM and wireless communications. However, as shown in Table 4, the high dynamic range comes at the expense of higher power consumption and a larger chip area. This suggested that log-amp limiters power detectors are less suitable for applications requiring small-chip areas and low power operation for days. In contrast, Table 4

also demonstrates that the differential structure design methodologies offer a dynamic ranging between 20 dB to 27 dB and a much smaller chip area. The power consumption is also relatively low, making them suitable for RF transmitters and communication receivers. As shown in Table 4, a distributed power detector can provide a wide operating frequency and low power consumption. Wide operating frequency is helpful in various applications involving wireless communications. Table 4 also shows that RMS power detectors have relatively low power consumption, low chip area, and reasonably high dynamic range, making them appropriate for different applications.

Table 4: Comparison between different existing power detector architecture

Reference	**Topology**	**CMOS Technology (nm)**	**Operating Frequency (GHz)**	**Dynamic Range (dB)**	**P_{DC} (mW)**	**Sensitivity (dB)**	**Chip Area (mm^2)**	**Applications**	**Date Published**
(Wu et al. 2011)	Log-Amp limiter	180	0.1 – 8.0	40.0	70.00	-	0.9800	GSM and AGC	2006
(Zhou & Chia 2008)	Differential	130	0.1 – 8.5	20.0	0.18	-	0.0126	RF transmitter	2008
(Valdes-Garcia et al. 2008)	Limiter and rectifier	350	0. 9 – 2.4	30.0	8.60	-	0.0310	RF measurements	2008
(Li, Gong & Wang 2010)	Differential	130	0.8 – 8.5	27.0	0.1	-	0.0850	Reflectometer and communication receiver	2010
(Sakphrom & Thanachayanont 2012)	Differential/ Log-amp limiter	180	0.5 – 3.0	50.0	0.90	-	0.0078	Wireless sensor network and telemetry	2012
(Xu et al. 2014)	Differential	65	0.1 – 44.0	20.0	-	-	-	Microwave and millimetre wave	2014
(Wang et al. 2015)	Limiter and rectifier	180	0.3 – 10.0	42.0	0.55	-	0.1130	Wireless communications	2015
(Choi et al. 2016)	Squaring cell	28	0.7 – 4.0	40.0	5.80	-	0.1499	RF transmitters	2016
(Qayyum & Negra 2017a)	Single FET	65	0.1 – 110	-	0.03	67	0.0096	Radio	2017

(Qayyum & Negra 2017b)	Distributed	130	7.0 – 70.0	30.0	0.16	75	0.0684	Wireless communications	2017
(Li et al. 2019)	Diode-Based	65	4.0 – 6.0	32.0	0.70	-	0.0036	Wireless Microwave power transfer	2019
(Yijun & Wah 2006)	Log-Amp limiter	130	2.0 – 16.0	45.0	35.20	-	-	GSM	2019

2.7. Conclusion

This chapter has explored the fundamentals of RF power measurement and the importance of RF power detectors' performance parameters. A brief overview of the different types of RF power detectors and their applications is also covered. The advantages and limitations of each design strategy were depicted, and a critical review was presented. From the critical review, it can be established that thermal detection, peak detection, squaring cells, and distributed power detectors are not suitable for this research, as it is complex to generate linear-in-decibel output. Schottky diodes are proper for low power applications, but their inaccuracy and instability at high-frequency range are not appropriate for this study. One possible implementation is a differential structure using MOSFET along with an exponential generator to generate linear-in-decibel output. However, the low dynamic range of exponential generators makes this implementation inadequate for our study. Another method is using logarithmic amplifiers along with rectifiers to produce linear-in-decibel output and wide dynamic range. The major disadvantage of this methodology is the relatively higher power consumption compared to the other power detector designs presented in this section. Therefore, for this study, a differential MOSFET structure is employed for microwave power detection together with an SDLA logarithmic amplifier to further amplify the signals and provide linear-in-decibel output. Since the output voltage of the differential power detector used to perform power detection is DC, no rectifiers are required reducing the power consumption considerably. Moreover, considering that low cost and low power consumption are major requirements for this project, the 180 nm CMOS technology is preferred as a trade-off between feasibility, cost, and power consumption.

Chapter 3

Power Detector Design Specifications

This section performs the 180 nm CMOS DC characterization to better understand the critical fundamentals characteristics and establish the power detector's specifications to meet application requirements. The power detector employed in this project focuses on low power consumption, wide dynamic range, and low sensitivity. Therefore, design trade-offs are required between the critical RF power detector parameters to meet all operating conditions requirements.

3.1. CMOS Inverter Characterization

The CMOS inverter is the fundamental block employed for IC design using CMOS technologies. CMOS inverter offers low power dissipation at relatively high speed (Sharma & Soni 2010). In addition, the large noise margin in both high and low states gives the CMOS inverter excellent logic buffer characteristics (Bae 2019). Presently, the advantages of the CMOS inverter offer IC designed in CMOS technologies the edge compared to other technologies. Figure 25 shows the circuit configuration of the CMOS inverter.

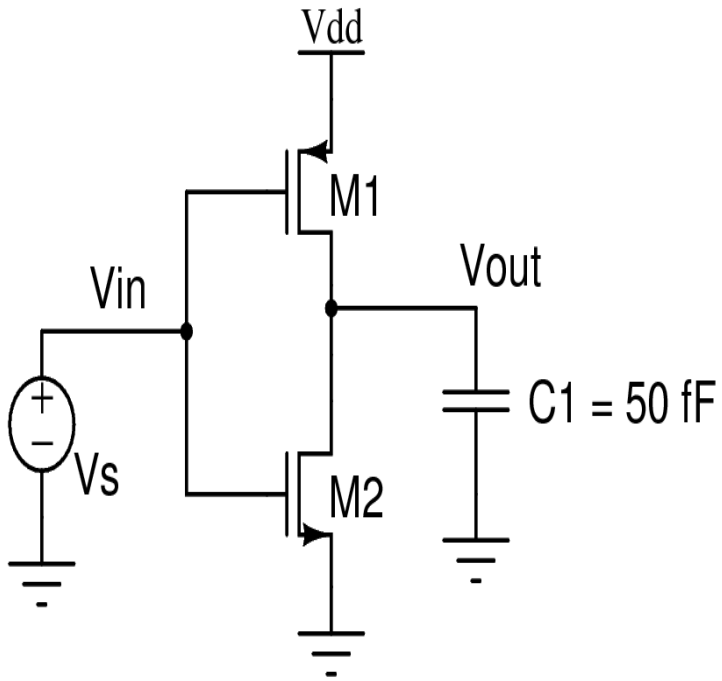

Figure 25:The CMOS inverter

As shown in Figure 25, the CMOS inverter comprises an NMOS and PMOS transistor connected at the gate and the drain terminal. The NMOS source terminal is connected to the ground, and the supply voltage V_{dd} is applied to the PMOS source terminal. A supply voltage V_{dd} of 1.8 V was employed, which is the standard for the 180 nm CMOS process. The input voltage V_{in} is applied to the gate terminals, and the output voltage V_{out} is connected to the drain terminals through a load capacitance C_L of 50 fF. The output load capacitance comprises the interconnect capacitance, the inverter drains junction, and the gate capacitances of fanout gates. The sum of the PMOS and NMOS transistor gate-to capacitances comprising the gate-to-channel capacitance and gate-to-drain overlap gives the gate-drain capacitance C_M of the CMOS inverter (Bisdounis, Nikolaidis & Koufopavlou 1998; Weste & Harris 2015). The W/L ratio of the NMOS and PMOS transistor is 0.18 µm/0.4 µm and 0.18 µm/0.8 µm, respectively.

Characterization of the CMOS inverter is crucial for accurate and high-performance design. The CMOS inverter DC and transient characterization using 180 nm CMOS process parameters were carried out to analyze critical parameters such as power consumption, leakage current, and propagation delay. The CMOS inverter leakage current is a major design consideration as it results in static power dissipation, which can become dominant in sub-micron CMOS (Bisdounis, Nikolaidis & Koufopavlou 1998). The leakage current comprises sub-threshold currents and reverse-bias diode current. The former is caused by carrier diffusion between the drain and the source of the off transistors, while the latter results from stored charges between the bulk and drain of the active transistors (Sharma & Soni 2010).

A DC simulation was run where the input source voltage V_s was varied from 0 V to 1.8 V to analyze the CMOS inverter leakage current, propagation delay, and power dissipation. Figure 26 shows a plot of the input voltage V_s (green), the CMOS inverter transfer characteristics (blue), and the current through the PMOS transistor (red). The leakage current is obtained at input voltage levels when both PMOS and NMOS devices have an opportunity to be in both on and off states. The simulated leakage current of the CMOS inverter due to the NMOS and PMOS transistor is 55.3 pA and 4.5 pA, respectively. Figure 26 also shows that the maximum short circuit current of the CMOS inverter is 53 µA. Furthermore, the CMOS inverter's maximum short-circuits power is equivalent to the area under the curve shown in Figure 26 (red).

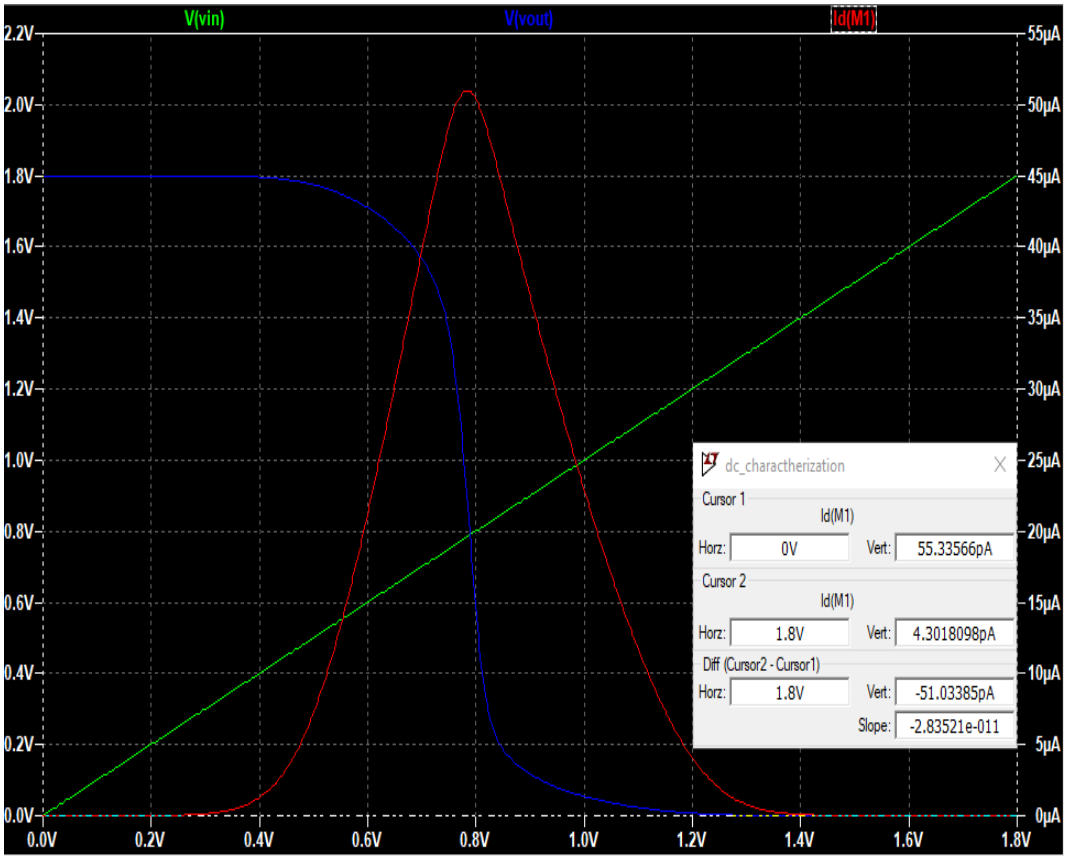

Figure 26: DC characterization of the CMOS inverter

The transient response and propagation delay of short channel devices are major performance metrics in digital CMOS. Therefore, a transient simulation was also performed by applying a pulse voltage to the gate terminals to analyze the transient response of the CMOS inverter. Figure 27 shows the transient response of the input and output voltage of the CMOS inverter. From Figure 27, the simulated propagation delay of the CMOS inverter when the input signal goes from low to high and vice versa at 50% voltage level is 175 pS. Figure 28 shows the instantaneous power dissipation of the NMOS transistor (green), the PMOS transistor (blue), and the CMOS inverter (red). From Figure 28, the average computed power consumption of the NMOS transistor, the PMOS transistor, and the CMOS Inverter is 4.34 µW, 4.31 µW, and – 8.45 µW, respectively.

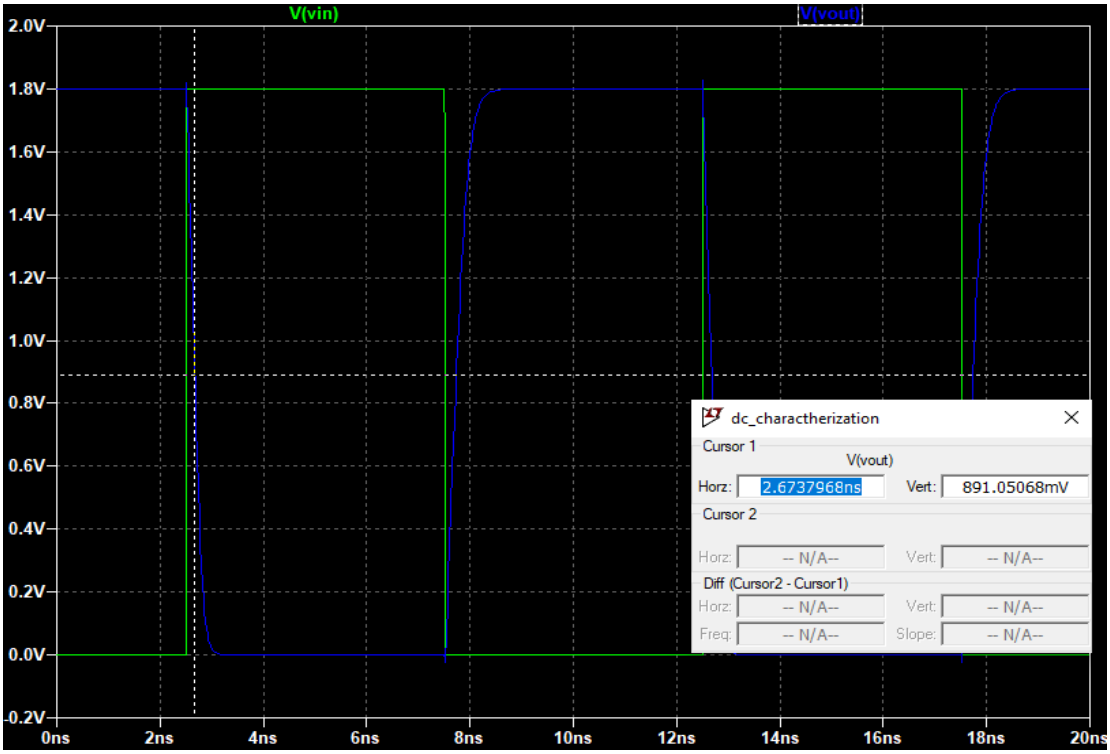

Figure 27: The CMOS inverter input and output voltage transient response

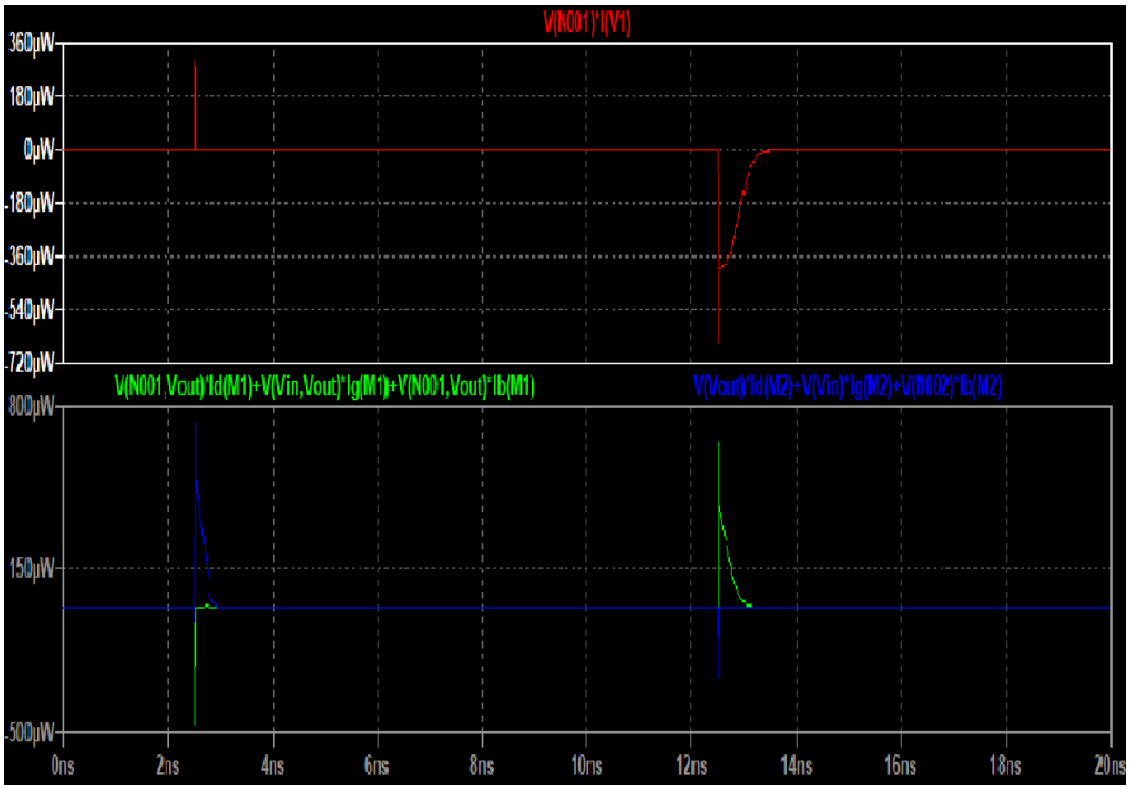

Figure 28:Power consumption of the NMOS, PMOS, and the CMOS converter

The DC characterization of the CMOS inverter using the 180 nm process parameters has now established the value of the critical parameters such as propagation delay, power dissipation, and leakage current. The proposed RF power detector parameters are also specified in the following sub-section before proceeding with the schematics design.

3.2. Parameters

3.2.1. Frequency Range

This research accentuates applications in the S-band frequency range, which, as designated by the Institute of Electrical and Electronics Engineers (IEEE), is from 2-4 GHz of the microwave band of the electromagnetic spectrum. The S-band range's 2-4 GHz region is utilized for wireless network equipment compatible with IEEE 802.11g and 802.11b standards (Sunghyun & Pavon 2003).

3.2.2. Dynamic Range

A wider dynamic range offers more flexibility for other system components selection, i.e., the directional coupler. Regarding this study, to satisfy the operating conditions and application requirements, a dynamic range of around 40 dB along with a maximum allowed error of ±2 dB is adopted. This dynamic range of 40 dB is achieved through the successive detection logarithmic amplifier. This successive detection logarithmic amplifier will also generate a linear-in-decibel output that can accommodate a wider dynamic range of frequency compared to a linear scale, as shown in Figure 29.

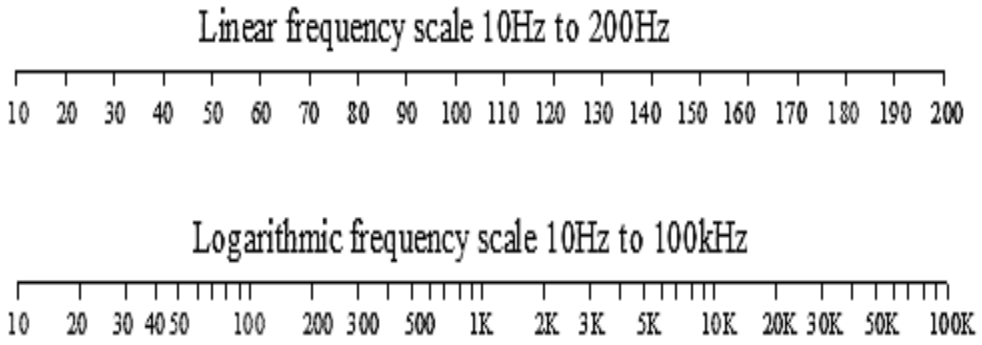

Figure 29: Linear and Logarithmic Scale Comparison

3.2.3. Input Power Range

The power detector input power range is commonly determined by the coupler coupling factor and the maximum output power amplifier. In this case, if the detector is connected to a coupler, the input resistance of the power detector should be 50 Ω. This project's applications involve power detection at low input power levels, so a suitable range is -50 dBm to 0 dBm.

3.2.4. Relative Power Accuracy

The relative power accuracy determines the power detector response at the input to a predefined power step for each operating condition. The operating conditions are not expected to change during the power step. Generally, the 1 dB power step and the 10 dB power step are critical for applications in the power control loop (Devices 2004). Regarding this project, the focus will be on the 1 dB step, which is the most critical requirement. The power detector relative power accuracy specification for the 1 dB power step is ±0.25 dB.

3.2.5. Operating Temperature

The operating temperature for IC design, including power detectors, are usually classified into the military (-55 °C to +125 °C), Extended (-40 °C to +125 °C), Industrial (-40 °C to +85 °C), and Commercial (0 °C to +85 °C). Generally, the bottom end of this range is not as important in comparison to the top end as the chip temperature will tend to increase due to the self-heating of the different active and passive components. Depending on the power detector's application, the top end can be extended to a higher temperature. However, the commercial temperature range of 0 °C and +85 °C is suitable for our application requirements for this study. Temperature variations should be optimized to minimize their effect on the operation of the device.

3.2.6. Power Supply

The power supply involving CMOS technology designs depends on the technology node employed, particularly in the case of P-spice simulation. Concerning this study, since the 180 nm standard CMOS technology is employed, the power supply is set to 1.8 V. For circuit design implementation, the fabricated chip should still operate normally for a supply voltage range between 1.6 to 2.0 V, which is the standard. The supply current can be up to 1.0 mA amid active operation.

3.2.7. Specifications Summary

Table 5: Specification summary for the power detector

Parameter	*Min*	*Typ*	*Max*	*Unit*
Operating Frequency f	2		4	[GHz]
Dynamic Range DR		40		[dB]
Input Power P_{IN}	-50		0	[dBm]
Relative Power Accuracy For 1 dB Power Step		±0.25		[dB]
Operating Temperature T	-0		85	[°C]
Supply Voltage V_{DD}	1.6	1.8	2.0	[V]
Supply Current I_{DD}			1.0	[mA]

3.3. Conclusion

In this chapter, the DC characterisation of the 180 nm CMOS inverter was evaluated to establish its leakage current, propagation delay, and power consumption. The CMOS inverter's critical performance parameters will improve our understanding of the 180 nm CMOS inverter fundamental characteristics are achieved, leading to a more accurate design. The design specification of the proposed RF power detector to meet all applications requirements under all operating conditions is also established. Since the RF power detector design specification is established, we can proceed with the circuit design and implementation.

Chapter 4

Methodology

This chapter presents the circuit configuration, design considerations, and schematics capture simulations of the proposed RF power detector. Firstly, the block diagram and the architecture of the RF power detector are described in detail. The RF power detector employs an RMS detector to perform power detection using MOSFET square-law characteristics in the strong inversion region. The circuit implementation of the RMS power detector and how power detection is achieved are depicted. Then the operation and structure of the successive detection logarithmic amplifier are thoroughly explained through stepwise mathematical analysis. The RF power detector core component, including the wideband input matching, the offset cancellation circuit, and the biasing circuits design, is also elaborated. The circuit configuration is analyzed, and operations are verified through system-level verification simulations.

4.1. Design Conceptualization

The design of an RF power detector for applications in wireless communication and as sensing devices in the agriculture sector is developed. The RF power detector should operate from 2 GHz to 4 GHz to target the S-band frequency range. Since RF signals involved in the targeted applications have a wide input dynamic range, linear-in-decibel characteristics are preferred to compress the signals into a smaller range. Furthermore, as the RF power detector will operate for days without battery replacement, minimum power consumption is also a significant design consideration. Several RF power detectors have been designed and fabricated during the past decades, with most being tested for dynamic range, sensitivity, and operating frequency range, as depicted in section 2.4. Each design topologies displays its advantages and limitations. This study employs MOSFET, square-law characteristics, and logarithmic amplifiers to design a linear-in-decibel RF power detector using CMOS technology.

Presently, with the continuous downscaling of CMOS technologies, the design of accurate and high-performance analog and RF integrated circuits has become very challenging (Razavi 1999). Furthermore, since the supply voltage of deep submicron technologies decreases faster than the threshold voltage of transistors, trade-offs between performance metrics have become more

complex. The 180 nm CMOS standard process is utilized in this research as a trade-off between complexity and feasibility. Even though several new CMOS technologies are available presently, the 180 nm node is preferred as it is well established for RF integrated circuit design. The RF power detector CMOS circuit design process includes defining circuit inputs and outputs, mathematical analysis and calculation, circuit simulations, layout design, parasitics extraction, and chip fabrication and testing. Figure 30 shows the flowchart representing the RF power detector design process flow in CMOS technology from top to end. Depending on the design and other significant factors such as cost, the flowchart may change slightly. A successful design should meet all the specifications as set in section 3.2.

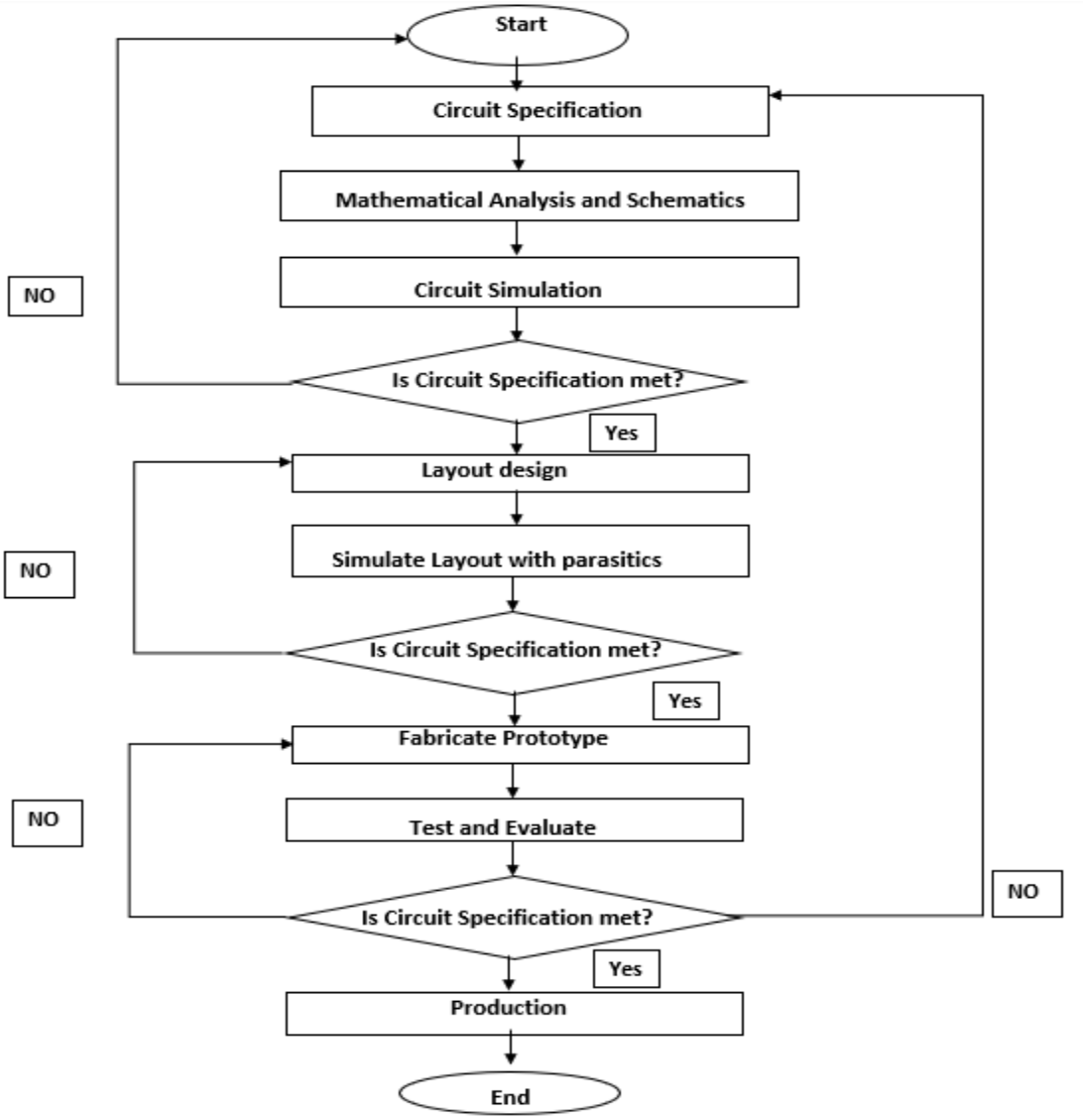

Figure 30: Flowchart displaying design conceptualization.

4.2. Block Diagram

The block diagram of the proposed linear-in-decibel RF power detector is illustrated in Figure 31. The RF power detector core blocks are shown in Figure 32 and depicted in detail from section 4.1-1 to section 4.1.5.

RF power detector major blocks lists:

1. Input Impedance Matching Block (section 4.1.1)
2. RMS Power Detector Block (section 4.1.2)
3. Successive Detection Logarithmic Amplifier Block (section 4.1.3)
    a. Limiting Amplifiers (section 4.1.3.4)
    b. DC Offset Cancellation Circuit (section 4.1.3.5)
4. Biasing Block (section 4.1.4)

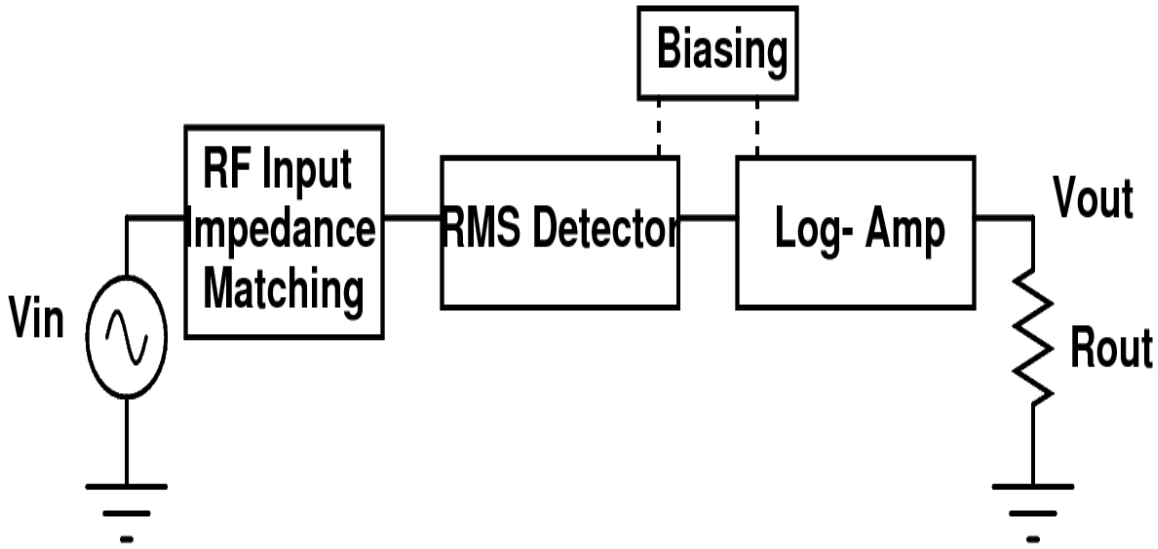

Figure 31:RF power detector block diagram

The RF power detector includes an RMS power detector unit, a DC offset cancellation circuit, and a five-stage successive detection logarithmic amplifier. The input RF voltage signal power is applied to the RMS power detector through a coupling capacitor and an impedance matching network. The coupling capacitor establishes an excellent common-mode for the RMS power detector block. The RMS power detector exploits the square-law characteristics of MOSFET operating in the saturation region to perform power detection. The five-stage logarithmic amplifier then further amplified the DC output voltage of the RMS power detector. The

successive detection logarithmic amplifier comprises cascaded limiting amplifiers realized using a Piecewise Linear Approximation. Linear-in-decibel output voltage is achieved through the compression of the input signal dynamic range. The limiting amplifiers each generate a differential output current and voltage. The differential output voltage is passed to the succeeding limiting amplifier while the differential output currents are summed and applied to resistors (Rs) to generate the output voltage. Rectifiers usually required for logarithmic amplifier design are omitted since the logarithmic amplifier input is a DC voltage. An offset subtractor is employed in a feedback loop to remove offset voltage. A first-order low pass filter which consists of MOSFET R_f and capacitor C_f is used to extract the DC output voltage. The dynamic range may be extended, with a greater number of stages at the expense of higher power consumption. This research employed a five-stage logarithmic amplifier as a trade-off between dynamic range, linearity, and power consumption.

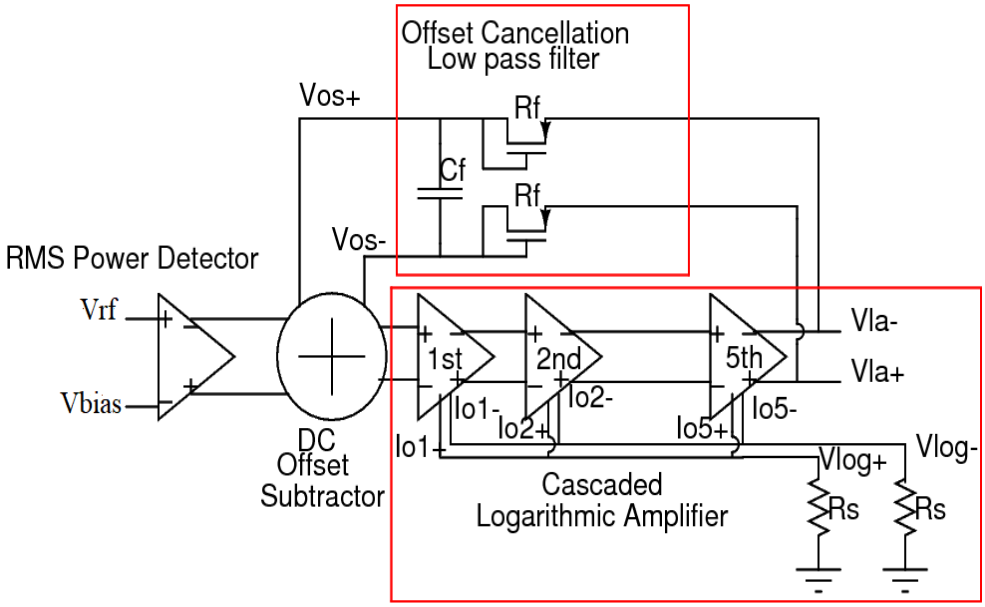

Figure 32: Block diagram RF power detector core

The power detector in this research is designed primarily for wireless communication and RF measurements in the agricultural sector. As such, the primary concerns are low power consumption, low sensitivity, and wide dynamic range. Therefore, the proposed circuit configuration is chosen to meet design specifications and applications requirements. In the following sub-sections, each circuit component of the RF power detector architecture is described thoroughly.

4.3. Circuit Configuration

In this sub-section, the circuit configuration of each major of the RF power detector is depicted in detail, along with mathematical analysis and circuit-level simulations.

4.3.1. Input Impedance Matching

Implementation Matching circuits are critical for microwave integrated circuit design to improve impedance mismatch between components, thus maximizing power transfer (Liao, Li & Li 2017; Stärke et al. 2017). Power detectors with a wide input matching frequency range simplify circuit design. Furthermore, the input matching circuit reduces the variations of the power detector's reflection coefficients and output voltage with frequencies. A simple RLC circuit was employed to realize wideband input matching with main objectives low power consumption and reduced chip area. Lumped elements C_1, C_2, C_3, L_1, and R_1, are adopted to design the impedance matching circuits. Lumped elements are considered a single-frequency matching process (Wang & Cao 2019). The tradeoffs that require further consideration when designing impedance matching circuits are matching region, gain, Noise Figure, and insertion loss. Figure 33 shows the small-signal equivalent circuit structure used to achieve wideband input matching. This wideband input matching may be represented by a second-order equation as follows

$$T(S) = \frac{a_2 S^2 + a_1 S + a_0}{S^2 + SB + {\omega_o}^2} \tag{4.1}$$

Where a_1, a_2, a_0 are the numerators' coefficients, B is the bandwidth, and **ω**o is the pole frequency of the system.

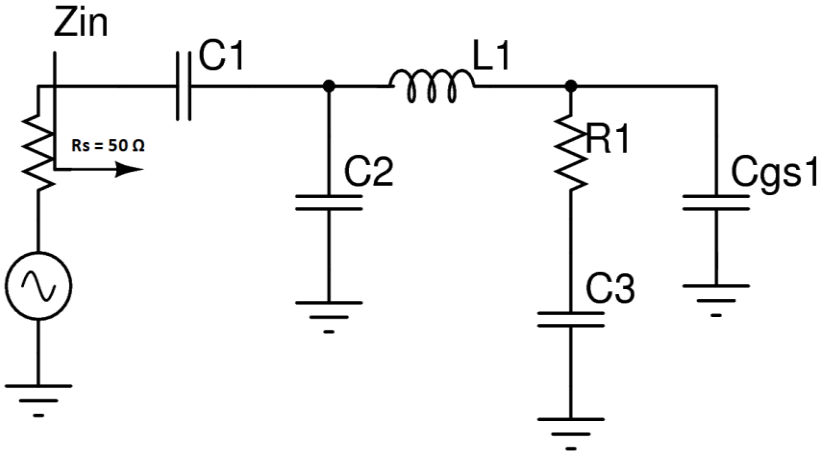

Figure 33: Wideband input matching small-signal equivalent (Chen 2013)

The RLC input impedance can be expressed as (Chen 2013)

$$Z_{in} = \frac{1}{SC_1} + \frac{1}{SC_2} // [SL_1 + (R_1 + \frac{1}{SC_3}) // \frac{1}{SC_{gs1}}] \quad (4.2)$$

$$= R_{in} + jX_{in}$$

Since the gate-to-source capacitance (C_{gs1}) is much smaller than the C_3, the expression (4.2) can be approximate as

$$Z_{in} = \frac{1}{SC_1} + \frac{1}{SC_2} // [SL_1 + (R_1 + \frac{1}{SC_3})], \quad (4.3)$$

$$Z_{in} \approx \frac{(S+(R_1/L_1))((C_1+C_2)/C_1C_2)}{S^2+S(R_1/L_1)+((C_2+C_3)/L_1(C_2C_3))} \quad (4.4)$$

In (4.3), a second-order expression is approximated for the RLC circuit, which implies roughly a second-order filter. The resonant frequency f_o and the quality factor Q of the RLC filter circuit are expressed by

$$f_0 \approx \frac{1}{2\pi}\sqrt{\frac{C_2+C_3}{L_1(C_2C_3)}} \quad (4.5)$$

$$Q \approx \frac{1}{R_1}\sqrt{\frac{L_1(C_2+C_3)}{C_2C_3}} \quad (4.6)$$

The performance of the input impedance circuit was verified with Computer-Aided Design (CAD) tools from Keysight ADS. From equations (4.5) and (4.6), a low-quality factor is required to achieve wider bandwidth. Wideband input matching can be realized by suitably choosing the values of the passive devices. In (4.6), R_1 is inversely proportional to the Q; therefore, R_1 is proportional to the bandwidth. L_1 is proportional to the quality factor and inversely proportional to the resonant frequency. Performance optimization tools available in the Keysight ADS software were also employed to compute the nominal values of the lump elements to meet this research specification and performance goals, thereby increasing the accuracy of the design. Several tradeoffs between bandwidth, noise figure, and wideband matching must be made, so the dimension of R_1, L_1, and C_3 must be chosen thoroughly. Table 6 shows the values of the passive devices employed in the input matching circuit after performance optimization using the Keysight ADS optimization CAD tools.

Table 6: Device size for the wideband input matching RLC circuit

Device	C_1 (pF)	C_2 (pF)	C_3 (pF)	L_1 (nH)	R_1 (Ω)
Size	10.0	0.1	9.6	1.0	50.0

Scattering Parameters The scattering parameters are critical parameters for microwave design, notably the S_{11} parameter, which indicates the input port voltage reflection coefficient. Figure 34 shows the simulated magnitude of S_{11} for the designed RF power detector shown in Figure 32. The input matching network was realized using lumped elements, as demonstrated in Figure 33. The simulated result shows that for the frequency range from 2 GHz to 4 GHz, the return is loss is better than -15 dB. A return loss of less than -15 dB is considered acceptable by industry standards. An example of the device size found in table 6 simulation optimization is provided in appendix A.

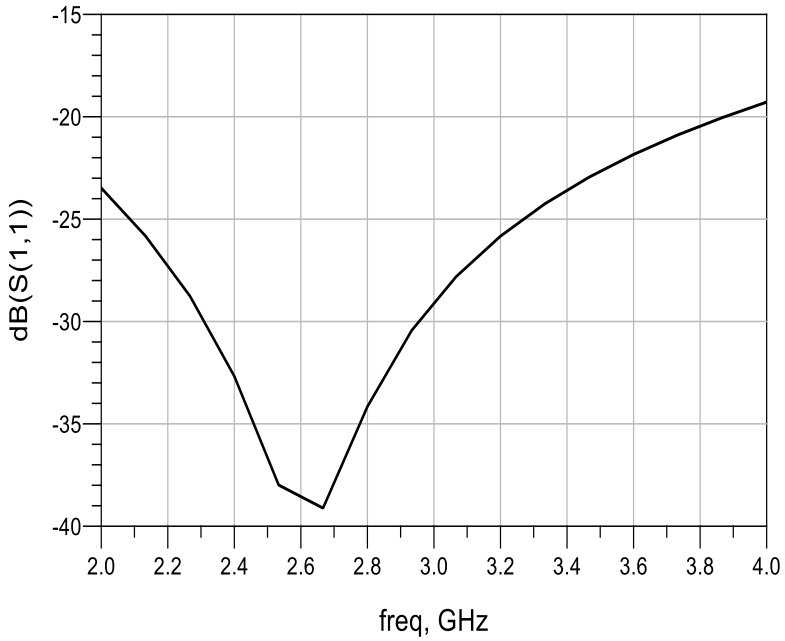

Figure 34: Simulated S_{11} magnitude for the input impedance matching circuit in Figure 32

Frequency Response The frequency response of the input impedance block was simulated, as shown in Figure 35. The frequency response has a high-pass characteristic with a + 20 dB/dec roll-off frequency. The high-pass corner cut-off frequency is approximately 1.5 MHz, meaning only 1.5 MHz to infinity signals can be allowed.

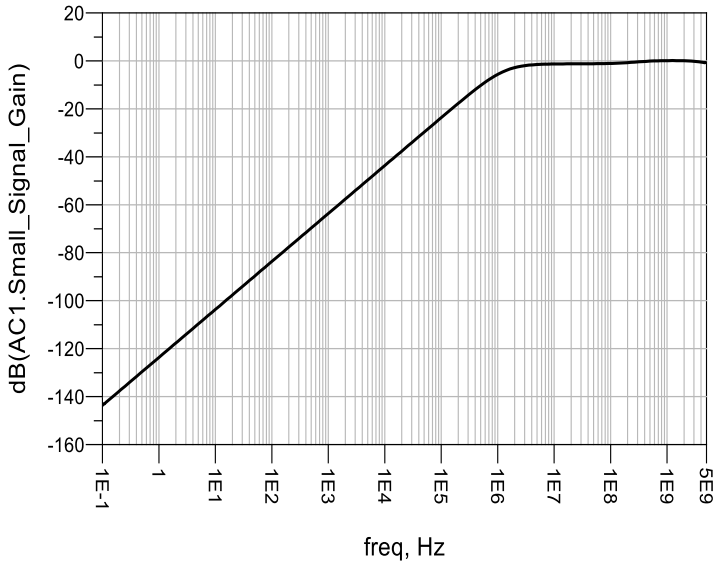

Figure 35: frequency response of the input impedance block

Monte Carlo Analysis A series of simulations were run to determine the effects of parameter mismatch and process variations on the input-matching S-parameter S_{11}. Figure 36 shows the Monte Carlo (MC) histogram simulated in Keysight ADS across 500 runs for the input-impedance matching when the input frequency is 2 GHz. The mean and standard deviation of the S_{11} parameter is -27.33 dB and 2.02 dB, respectively. It implies that the effect of parameter mismatch and process variations across 500 runs on the S-parameter S_{11} at 2 GHz is small, validating the input matching circuit robustness.

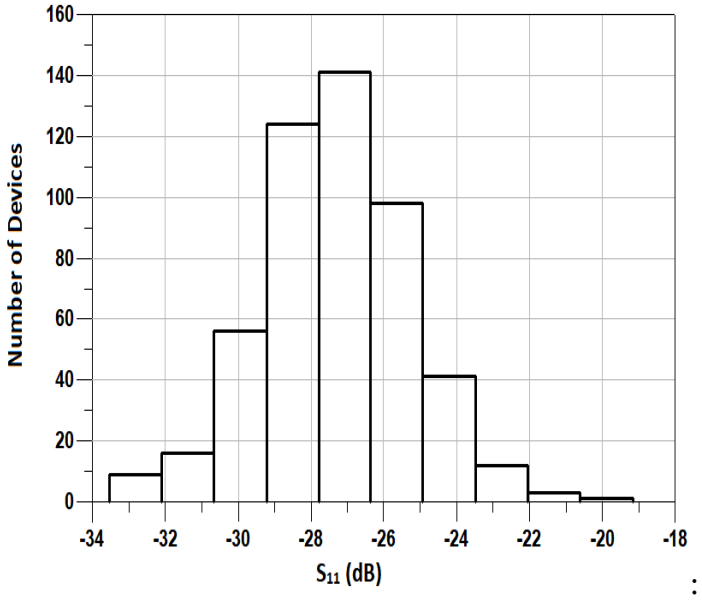

Figure 36: Monte Carlo simulation across 500 runs for S_{11} parameter at 2 GHz.

4.3.2. The RMS Power Detector

Implementation A cascode configuration with current-source load is employed to realize high sensitivity and high conversion gain. For wireless communication and RF measurements, good input sensitivity is a significant consideration. The power detector's new topology has a current source-load structure with a large gain that enhances input sensitivity. Furthermore, the current source-load structure offers high output resistance when the load has high resistance. Figure 34 shows a cascode configuration with a PMOS as current source along with its output equivalent circuit. Resistor R_{o1} represents the cascode stage output resistance while r_{o2} represents the PMOS output resistance. Since the output resistance, r_{o2} of the PMOS is much smaller than the cascode output resistance R_{o1}, the voltage gain of the cascode structure with PMOS as current source is given by

$$|A_V| = g_{m1}(R_{o1} // r_{o2}) \approx g_{m1} r_{o2} \tag{4.7}$$

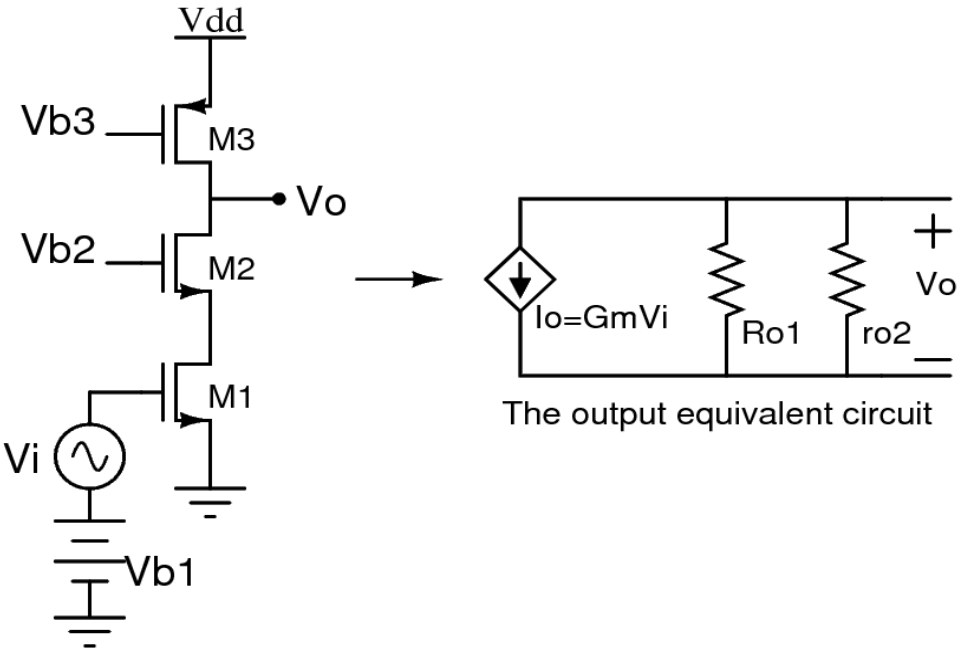

Figure 37: Cascode configuration with PMOS as current source

Figure 35 shows the proposed RMS power detector circuit configuration. BSIM3V1 was used to model the transistors using 180 nm CMOS process parameters.

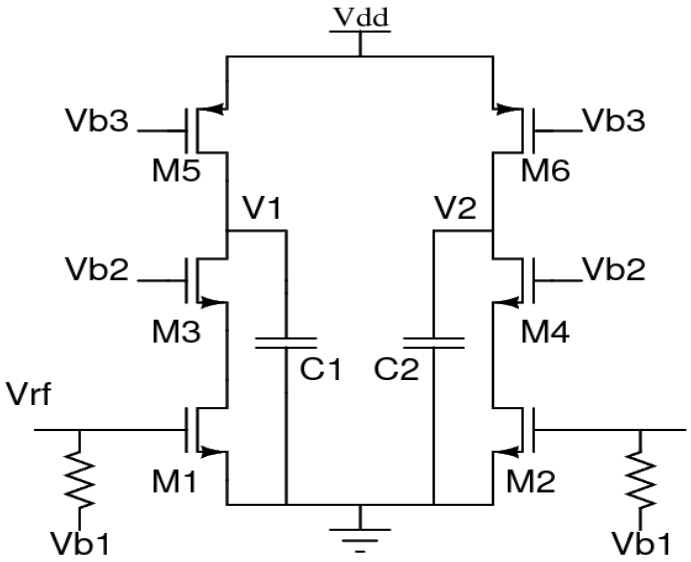

Figure 38: Proposed RMS power detector

The RF input signal is applied to the input transistor M_1 through an impedance matching network. The transistors M_1 and M_2 have the same W/L ratio and are biased in the strong inversion region with the same biasing voltages. The transistor M_1 is the main transistor generating the DC current proportional to the input power. This DC current contains the power information of the RF input signal. The square-law characteristics of MOSFET in the saturation region are exploited to perform power detection. The NMOS transistor M_3 also performs a similar function but as an auxiliary transistor. The auxiliary transistor creates additional intermodulation distortion components suppressing the third-order intermodulation (IM3) distortion by feed-forwarding to the output of each gain unit cell (Nguyen et al. 2020). The PMOS transistor M_5 acts as an active load enhancing the output sensitivity of the RF power detector. Smaller size for the PMOS load was used since the parasitic capacitance at the output node increased with the PMOS load size.

A differential structure reduces offset errors caused by the supply voltage and temperature variations (Yijun & Wah 2006). The drain current of the MOSFETs M_3 and M_4 may be expressed as

$$I_{DS3} = \frac{\mu n c_{ox} {}^{W}/_{L}}{2} (v_{RF} + V_{Bias} - V_{TN})^2 \quad (4.8)$$

$$I_{DS4} = \frac{\mu n c_{ox} {}^{W}/_{L}}{2} (V_{Bias} - V_{TN})^2 \quad (4.9)$$

V_{Bias} is the biasing voltage, L and W are the transistor's length and width, respectively. V_{TN} denotes the threshold voltage, C_{ox} and μ_n, the capacitance per unit area, and the average electron mobility. Assuming that the input signal $V_{rf} = V_i \cos(\omega t)$, hence the output voltage V_1 and V_2 can be derived as (4.10) and (4.11), respectively.

$$V_1 = V_{DD} - |V_{tp}| - (V_{GS} + V_{RF} - V_{TN})^2 \quad (4.10)$$

$$V_2 = V_{DD} - |V_{tp}| - (V_{GS} - V_{TN})^2 \quad (4.11)$$

From (4.8) and (4.9), the differential output voltage is expressed as

$$V_1 - V_2 = r_{out} X (I_{DS1} - I_{DS2})$$

$$= r_{out} \frac{\mu_n C_{ox} W}{2L} X \left\{\frac{1}{2}V_i^2 + \frac{1}{2}V_i^2 cos(2\omega t) - 2V_i^2 cost(\omega t)[V_{GS} - V_{TN}]\right\} \quad (4.12)$$

The alternating ground capacitors C_1 and C_2 act as low pass filters (LPF) and remove the output voltage's higher harmonics. A higher capacitance value for the alternating ground capacitance will better smoothen the differential output voltage at the expense of decreasing the differential output voltage. A capacitance of 0.1 pF was utilized for C_1 and C_2 for the proposed design. The major limitation of the proposed circuit configuration for the RMS power detector is the low voltage output swing. Therefore, extra care must be taken when choosing the transistor size and biasing voltage to optimize voltage headroom. The RMS power detector differential output voltage is given by equation (4.13), which is proportional to the RF input signal amplitude square.

$$V_1 - V_2 = \frac{\mu_n C_{ox} W}{4L} r_{out} V_i^{\,2} \quad (4.13)$$

Hence, as described in (4.13), the output voltage of the RMS power detector contains the input power information. With the continuous downscaling of MOSFETS, the short channel effect velocity saturation can become significant. Velocity saturation can cause MOSFETs to deviate from the square-law principles and become linear. Henceforth, including short channel effect velocity saturation, the I-V characteristics of MOSFETS can then be expressed as (Gray 2009)

$$I_{DS} = \frac{C_{OX}\,\mu_n}{2}\frac{W}{L}\,(V_{DS(act)})^2 \quad (4.14)$$

where $V_{DS\,(act)}$ is the minimum value of V_{DS} in the presence of velocity saturation of MOSFETs, at which the saturation region begins. $V_{DS\,(act)}$ can be expressed as

$$V_{DS(act)} = \varepsilon_c L\left(\sqrt{1+\frac{2(V_{GS}-V_t)}{\varepsilon_c L}}-1\right) \tag{4.15}$$

where E_c is the critical field value at which velocity saturation happens and (4.14) can be expressed as

$$I_{DS} = \frac{C_{OX}\,\mu_n}{2}\frac{W}{L}\,(V_{GS}\,-\,V_t)^2\left(1-\frac{V_{GS}-V_t}{EcL}+\cdots\right)$$

Therefore, including short channel effect velocity saturation, thus, (4.13) becomes

$$V_1 - V_2 = \frac{\mu_n C_{ox} W}{4L} r_{out} V_i^{\,2}\left[1-\frac{3(V_{GS}-V_t)}{EcL}+\cdots\right] \tag{4.16}$$

From (4.16), it can be established that the differential output voltage still contains the RF input information even though the short channel effect exists.

The minimum detectable input power of the RMS power detector is established by the input noise voltage of the circuit (Yingbo et al. 2012). So, given that the input noise voltage is V_n (nV/√Hz), the minimum detectable input power is given by

$$P_{n|dBm} = 10\,lg\left[\int_0^{\infty}\frac{V_n^2(f)}{R_s}df\right]+30 \tag{4.17}$$

where Rs represents the 50 Ω source impedance, and 30 is a constant representing the conversion ratio for dBm. Given that the noise bandwidth BW_n is established, equation (4.17) then becomes

$$P_{n|dBm} = 10\,lg\left(\frac{V_n^2}{R_s}BW_n\right)+30 \tag{4.18}$$

Thus, if the input noise of the RMS power detector is 4.0 nV/√Hz with a bandwidth of 1.0 GHz, the minimum detectable input power is -65 dBm. As such, since the input noise voltage of the RMS power detector establishes the minimum detectable input power, it is essential to optimize the design for minimum noise.

Transient Response Figures 39 (a), and 39 (b) show the transient response of the differential output voltage when there is no alternating capacitor C_1 and when alternating capacitor C_1 is 0.1 pF. As demonstrated in Figure 39 (a) and 39 (b), the alternating capacitor filters the differential

output signal and remove the higher harmonics to generate a quasi-DC signal. Increasing the value of the alternating capacitors, C1 will decrease the differential output voltage for fixed input power.

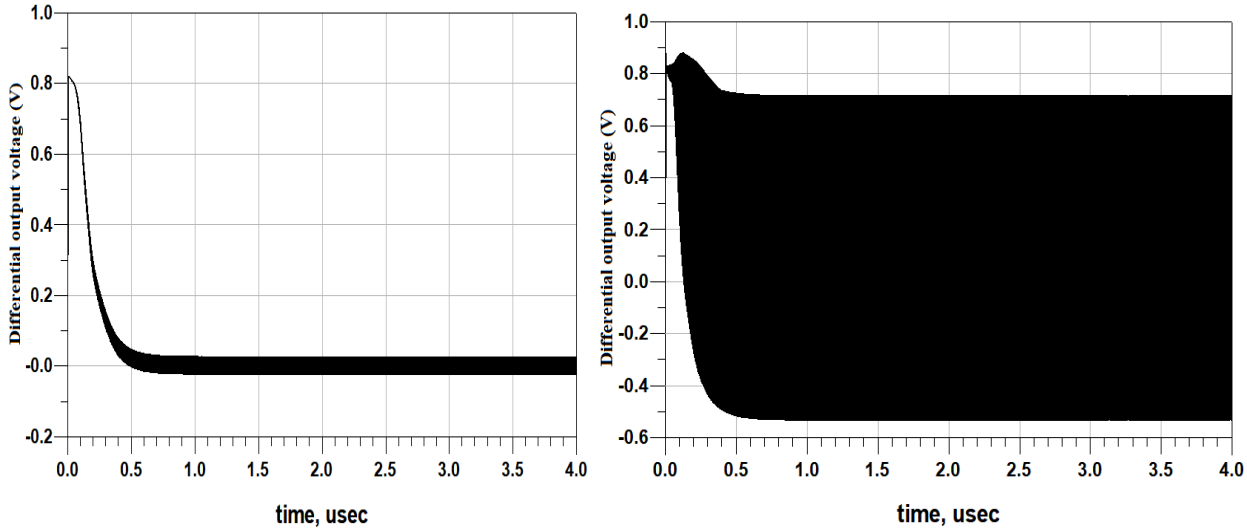

Figure 39: Transient response of the differential output voltage when (a) no alternating capacitor (b) when alternating capacitor C_1 is 0.1 pF

Harmonic Balance analysis The input-output characteristics of the RMS power detector were simulated at 2 GHz using Keysight ADS harmonic balance analysis. The simulated differential output voltage when the input power is swept from -100 dBm to 0 dBm at 2 GHz is plotted in Figure 40. As a comparison, the RMS power detector circuit employed in (Sakphrom & Thanachayanont 2012) was also designed and simulated using identical operating conditions and circuit parameters. The proposed RMS power detector has good linearity over the detection range (-100 dBm to -18 dBm), after which the RMS power detector enters into saturation. As shown in Figure 35, the proposed power detector achieves good sensitivity due to the high conversion gain. A significant advantage of the high conversion gain is that the following logarithmic amplifier design can be simplified. As shown in Figure 40, the RMS detector in (Sakphrom & Thanachayanont 2012) has a slightly wider input detection range and better linearity. This is mainly because of the lower voltage headroom of the cascode configuration, making the RMS power detector enters saturation for lower input power. However, better sensitivity and lower power consumption were simulated for the proposed RMS power detector.

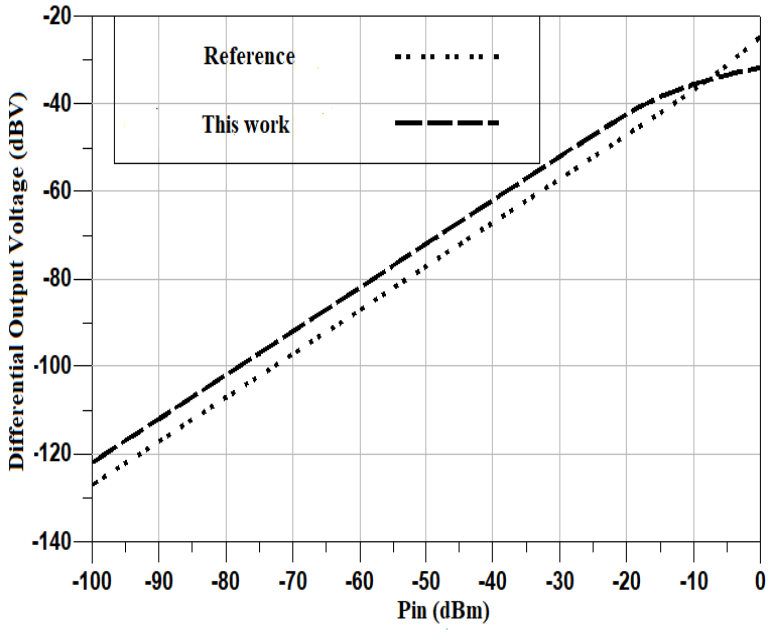

Figure 40: The differential output of the RMS power detector unit at 2 GHz

Noise Analysis Considering noise, Figure 41 shows the simulated Noise Figure (NF) of the RMS power detector over the frequency range of 2 GHz to 4 GHz. The simulated noise Figure demonstrates good noise performance of less than 4 dB over the frequency range of 2 GHz to 4 GHz.

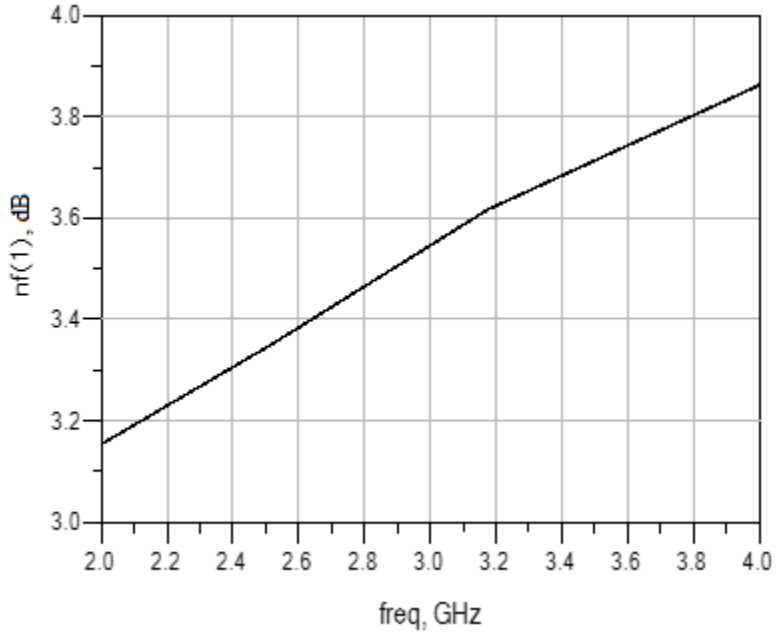

Figure 41: Noise Figure of the RMS power detector unit

As mentioned in (Zhou & Chia 2008), it is essential to note that this circuit configuration can still perform power detection despite short-channels effects and offset voltages. The transistors dimension for the RMS power detector is listed in Table 7.

Table 7:Transistor dimension for the RMS power detector

	W (µm)	L (µm)
M1, M2	3.2	0.18
M3, M4	0.4	0.18
M5, M6	0.4	0.18

4.3.3. The Successive Detection Logarithmic Amplifier

This section analyzes the operation of the successive detection logarithmic amplifier and their performance parameters, i.e., intercept and log slope. Additionally, the circuit implementation of the proposed successive detection logarithmic amplifier is depicted in detail. As mentioned previously, the logarithmic amplifier's main objective is to amplify further the DC output voltage of the RMS power detector and generate a logarithmic output voltage. Hence, it is essential first to comprehend how logarithmic output voltage is realized from the input signal.

Operation To have a clear overview of how linear-in-decibel output voltage is obtained from the RF input signal, let us analyze Figure 42, which illustrates a simplified logarithmic amplifier architecture.

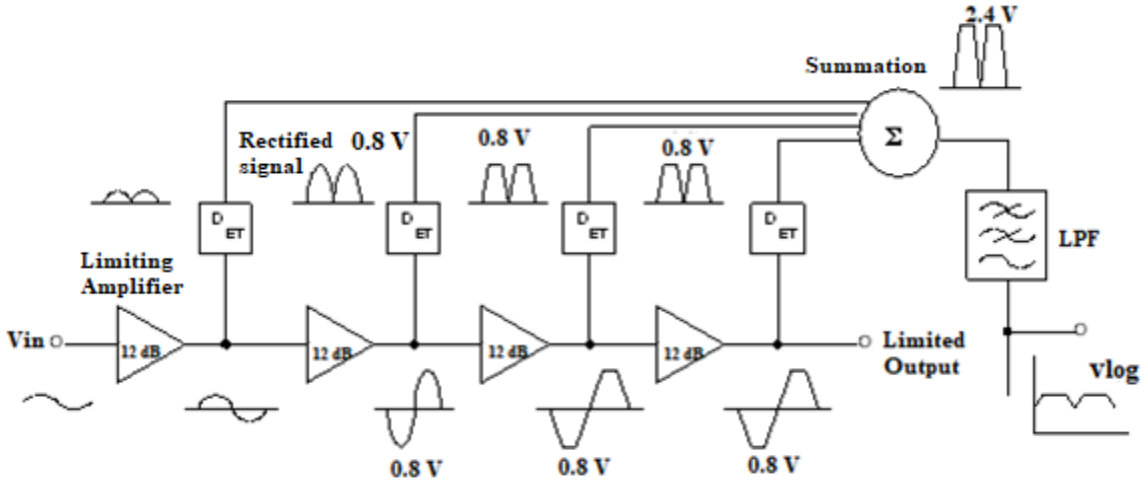

Figure 42: Logarithmic amplifier architecture

The log-amp comprises of four limiters, each having a gain of 12 dB (3.98x) which are limiting at a 0.8 V peak. From Figure 42, when a small sine wave voltage is applied to the input of the SDLA, the input signal is amplified by 12 dB at every gain stage. As the signal progress through the cascaded gain stages of the SLDA, at one instant, the signal will be greater than the 0.8 V limiting voltage. When this happens, the output voltage of that specific gain stage is the 0.8 V clipping voltage. Referring to Figure 37, this phenomenon occurs at the input of the third stage. Thus, a clipped signal is produced at the output of the third stage. Furthermore, since the third gain stage's output signal is sufficiently large to saturate the succeeding gain stages, their output signal voltage will also clip at 0.8 V. Consequently, as illustrated in Figure 42, we have two limiters with limited output voltage and two limiters with non-limited output voltage. Each limiter's output voltage is detected by full-wave rectifiers, summed, and averaged consecutively using a low pass filter.

For a clear understanding of the logarithmic amplifier linear-in-decibel characteristics, let us analyze the circuit when the input signal is decreased by 12 dB. Referring to Figure 42, the total output voltage at the summing device's output is a 2.4 V_{peak}. (from one limiter, which is about to limit, and two limiters which are already limiting). When the RF input signal is decreased by 12 dB, one less limiter is limiting. Consequently, the total output voltage of the summing devices drops to 1.6 V_{peak}. If the input signal further decreases by 12 dB, the summing device's output will reduce to 0.8 V_{peak}. Thus, the output voltage changes by 0.8 V for every 12 dB change in the RF input signal. As a result, we can conclude that the logarithmic amplifier has a log slope of 66.7 mV/dB, demonstrating its linear-in-decibel characteristics.

The Ideal Transfer Function The transfer function of a successive detection logarithmic amplifier is a fundamental characteristic. Figure 43 shows the ideal transfer function of an SDLA where V_{IN} denotes the input voltage, and V_{OUT} represents the output voltage. The input signal voltage is in the logarithmic domain on the X-axis. From Figure 43, it is demonstrated that the V_{OUT} increases linearly with V_{IN} (dB) over a range where V_Y is the log slope. V_X is the intercept voltage that occurs when $V_X = V_{IN}$. (It is important to note that for a real log detector, the transfer function will never cross the X-axis). V_X is a critical parameter since the actual RF input level is determined using V_X (Devices 2008). The linear-in-decibel relationship between the RF input signal and the output voltage makes the output interpretation simpler.

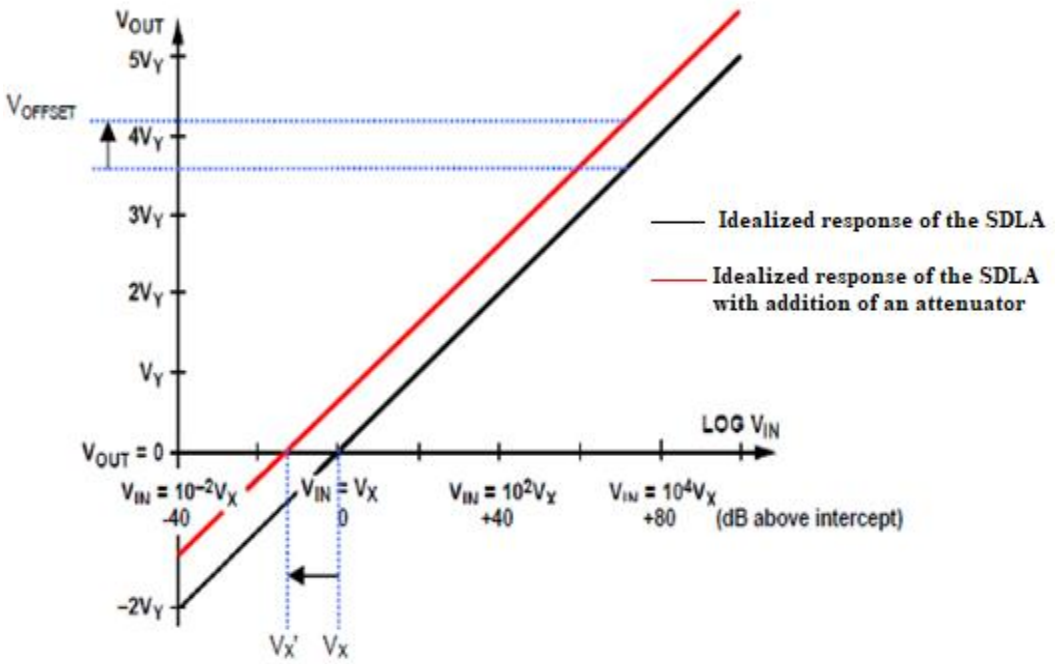

Figure 43: SDLA ideal transfer function (Bleeker 2012)

The relationship between the output and the input signal when the variables are voltages is expressed as

$$V_{log} = V_Y . \log\left({V_{in}}/{V_X}\right) \tag{4.19}$$

where V_Y is the slope in volt/decade, and V_X is the y-intercept. From (4.19), we can clearly establish that the two reference variables V_Y and V_X, are required to scale the output voltage. This suggests that the accuracy of the logarithmic amplifier depends on the precision of these two fundamental parameters.

It is important to note that the linear amplifier transfer function differs from a logarithmic amplifier, as in (4.19). From the derivative of (4.19), where the logarithmic base is δ, the gain of the SDLA becomes

$$\frac{\delta V_{OUT}}{\delta V_{IN}} = \frac{V_Y}{V_{IN}} \tag{4.20}$$

The instantaneous value is inversely proportional to the incremental gain. This argument holds true for any other logarithmic base.

Furthermore, as illustrated in Figure 40, an attenuator's addition before the logarithmic amplifier changes the intercept at the input. However, the log slope of the logarithmic amplifier remains unchanged. As illustrated in Figure 40, the addition of an attenuator only shifts the detection range (Yingbo et al. 2012). This research utilizes this concept by placing an RMS power detector before the logarithmic power detector to enhance the sensitivity of the RF power detector.

Slope and Intercept The log slope is defined as the change in the output voltage per change in the input power. Figure 44 illustrates the transfer function of a real Logarithmic detector at -40 °C, 25 °C, 85 °C, and 125 °C for a frequency of 900 MHz (devices August 2017). For every 10 dB change of the input power, the output voltage changes by 180 mV over the linear operating range (- 70 dBm to 10 dBm). Henceforth, the logarithmic power detector transfer function slope is 18 mV/dB.

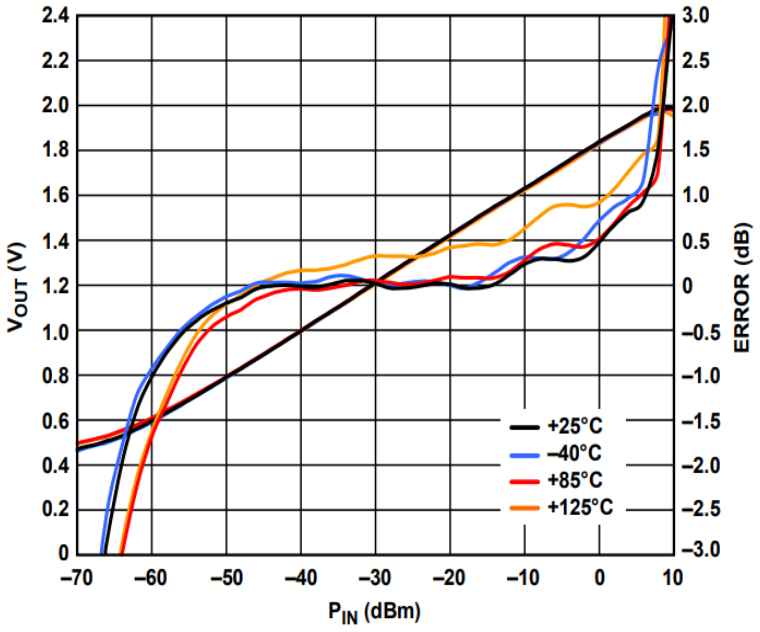

Figure 44: Real log detector transfer function (devices August 2017)

In previous sections, the Y-intercept of an ideal log detector was defined as the input power for zero output voltage. However, for real log detectors, this definition is no longer valid. From Figure 44, we can establish that the transfer function deviates from the ideal response at smaller input power values. As shown in Figure 41, the Y-intercept is instead an extrapolated point where the transfer function intersects the X-axis.

The non-ideal characteristics of the transfer function at smaller input power are because of the subsequent reasons. From equation 4.20, we noted that the instantaneous value is inversely proportional to the incremental gain. In the case of an ideal logarithmic amplifier, this implies that the gain would be infinite for infinitely small signals. However, this characteristic is not practical; thus, the transfer function's deviation happens for a real logarithmic amplifier. Since the logarithmic amplifier usually has a high gain, even if there is no input signal, the circuit's thermal noise will generate a finite output (Gilbert).

The logarithmic detector slope is calculated using a two-point calibration method that measures the output voltage for two unknown input power levels. In the linear operating range. The slope of the detector is expressed as

$$Slope = \frac{V_{OUT2} - V_{OUT1}}{P_{IN2} - P_{IN1}} \tag{4.21}$$

The X-intercept is determined using equation

$$P_{INTERCEPT} = P_{IN1} - \frac{V_{OUT1}}{Slope} \tag{4.22}$$

Once the logarithmic detector slope and intercept are established, we can predict the ideal output voltage for any input level inside the linear range of the device using the equation:

$$V_{OUT} = Slope\ X\ (P_{IN} - P_{INTERCEPT}) \tag{4.23}$$

A logarithmic power detector is typically used to estimate an unknown input power level from the measured output voltage linear range. Thus, using equation 4.22, an expression to determine input power from measured output voltage is given by

$$P_{IN} = \frac{V_{OUT\_MEASURED}}{slope} + P_{INTERCEPT} \tag{4.24}$$

Log conformance error The log-conformance is the difference between the power detector's measured and ideal transfer characteristics. This characteristic of logarithmic power detectors establishes their log linearity. By log linearity, the interest is actually on the transfer function conformance to the ideal log(x) mathematical function (Bleeker 2012). The log conformance error can be expressed as

$$error\ (dB) = \frac{V_{OUT,\ measured} - V_{OUT,\ ideal}}{slope} \tag{4.25}$$

$$= \frac{V_{OUT,\ measured} - slope(P_{IN} - P_{INTERCEPT})}{slope}$$

$$= \frac{V_{OUT,\ measured}}{slope} - P_{IN} + P_{INTERCEPT}$$

where *slope* is the change in output voltage divided by change in input power, P_{IN}. The $P_{intercept}$ is the calculated power in decibels (dB) when the output voltage is 0 V. The error curve represents the power detector accuracy and stability (Cowles 2004). It also demonstrates the range for which the logarithmic detector slope is constant. Furthermore, the log conformance error can investigate the power detector's linearity over changes in various environmental conditions. From Figure 45, the power detector linearity and transfer function are examined at -40 °C and 85 °C, then compared to room temperature performance. A log conformance error of ±2.0 dB is typically employed for the industry.

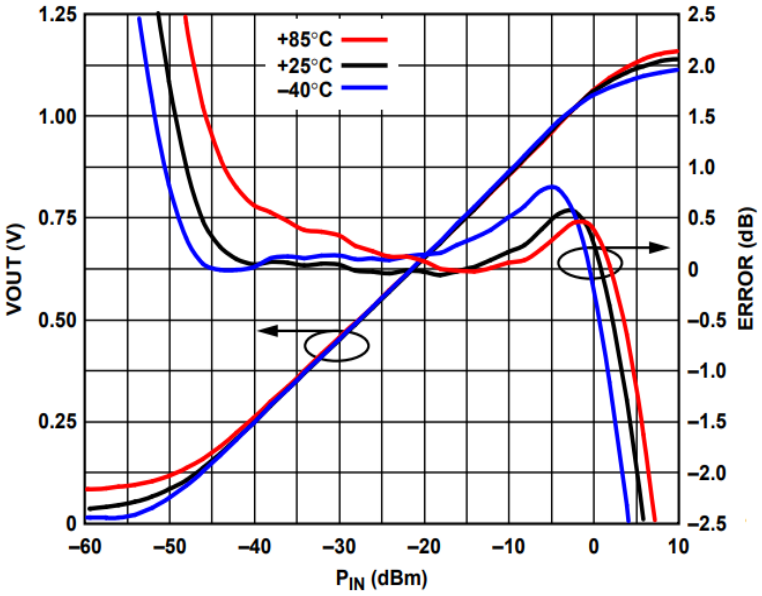

Figure 45: Response of a Logarithmic detector at higher frequencies (Devices. 2011)

The deviation of the transfer function from the ideal response for small signals is described in the prior subsection. At higher frequencies, the log detector transfer function also deviates from the ideal response. Some reasons for this deviation are non-ideal effects and the declining gain of the limiters at a higher frequency.

4.3.4. Circuit Architecture

Successive detection logarithmic amplifiers can be additionally classified into Piecewise Linear Approximation (PWL) and single-stage types. Single-stage types exploit the non-linear characteristics of PN-junction diodes or MOSFET operating in the subthreshold region to realize linear-in-decibel output (Sundarasaradula & Thanachayanont 2017). In contrast, PWL logarithmic amplifiers are more appropriate for high-frequency applications and consist of cascaded limiting amplifier stages to achieve the required logarithmic function. PWL implementations may be subdivided into parallel summation and series linear limits (Ramos et al. 2010; Sundarasaradula & Thanachayanont 2013). Series linear limits logarithmic amplifier comprises cascaded dual gain cells consisting of a unity-gain buffer parallel with a high gain limiting amplifier (Derafshi & Frounchi 2014). Parallel summation does not require a unity gain buffer, resulting in much lower power dissipation and chip area (Zareie, Hosseinnejad & Azhari 2019). Therefore, in this research, parallel summation is employed to design the logarithmic amplifier as compared to series linear limit architecture. Parallel summation may further be subdivided into two main architectures: progressive compression and parallel amplification (Bahrami & Shamsi 2015; Yong et al. 2009). Progressive compression parallel-summation architecture is employed to design the multistage stage logarithmic amplifier, and since its input voltage is DC, a wide bandwidth is not necessary.

Implementation Figure 46 shows a typical block diagram for an N-stage progressive compression parallel-summation logarithmic amplifier.

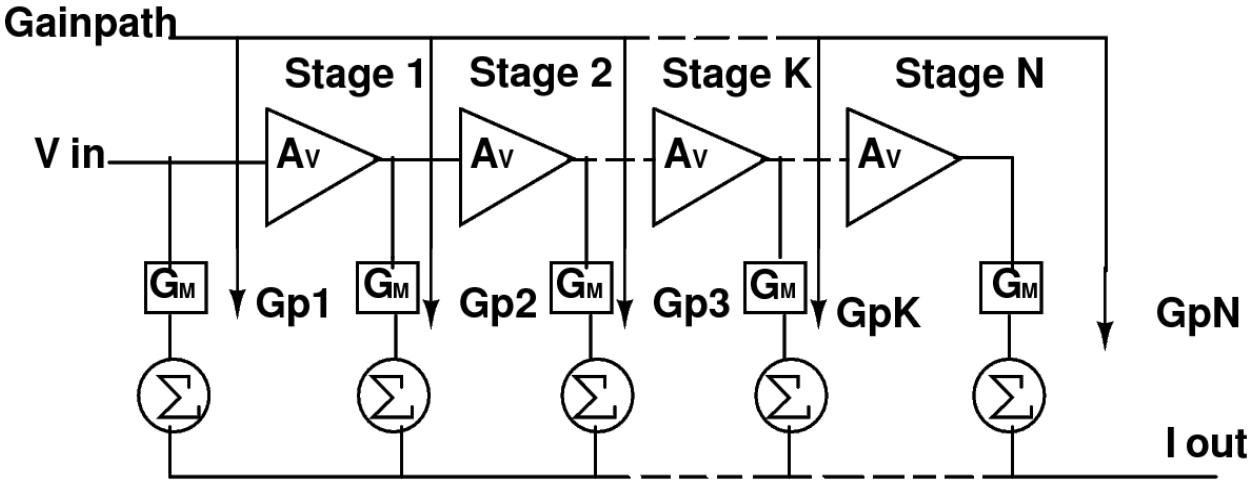

Figure 46: Conceptual progressive compression parallel-summation logarithmic amplifier

The transfer function of the parallel summation logarithmic amplifier shown in Figure 46 is illustrated in Figure 47. For progressive compression logarithmic amplifiers, a transconductance element converts the output voltage into current at each stage to a level that limits these currents.

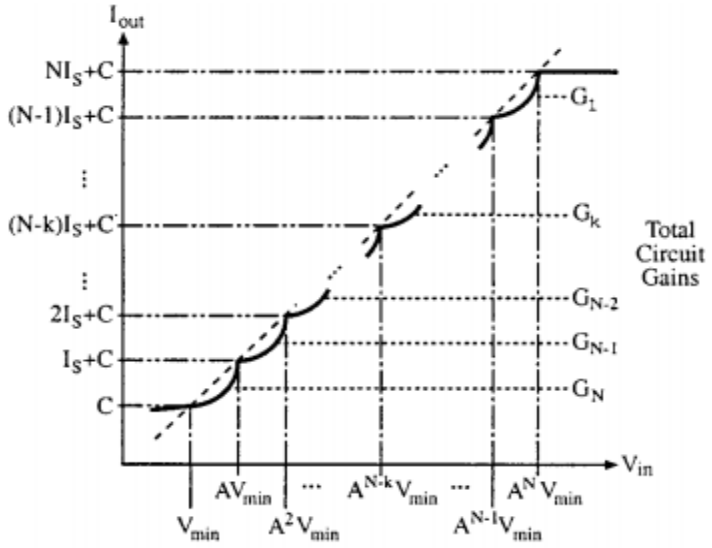

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Figure 47: Parallel-Summation logarithmic amplifier transfer function (Holdenried et al. 2002)

The current I_S and constant A from Figure 44 is the increased factor of the output current and input voltage at each stage of the logarithmic approximation. As shown in Figure 44, at any level, the overall output current comprises of a constant limited current provided by the gain paths and a current proportional to the input voltage. The overall gain G_k of the amplifier and the gain G_{pk} of each path k, where k = 1, 2, …, N may be expressed as

$$G_k = G_{p1} + G_{p2} + \cdots + G_{pk} = g_m A^{k-1} \tag{4.26}$$

$$G_{pk} = g_m A^{k-2}(A-1) \tag{4.27}$$

respectively. Furthermore, the input voltage may be expressed as (4.28), assuming that the k_{th} path shown in Figure 43 is about to start limiting.

$$V_{ink} = V_{in} = \frac{I_L}{G_{pk}} \tag{4.28}$$

From (4.27), it was found that $G_{pk} = g_m A^{k-2}(A-1)$, therefore V_{in} is rewritten as

$$V_{ink} = V_{in} = \frac{I_L}{g_m A^{k-2}(A-1)} \qquad \text{for } k \geq 2 \tag{4.29}$$

Considering that each segment's kth path is limiting, then there are N – k paths of greater gains that are also limiting and k – 1 additional path that are yet linearly amplifying. So, the overall output current of the logarithmic amplifier is given by

$$I_{out} = (N - k)I_L + [G_{P1} + G_{P2} + \cdots + G_{pk}]V_{in} \quad (4.30)$$

Substituting (4.26) and (4.27) into (4.28) gives

$$I_{out} = (N - k)I_L + \frac{AI_L}{A-1} \quad (4.31)$$

Furthermore, (4.29) may be rewritten as

$$K = log_A[\frac{A^2 I_L}{g_m V_{in}(A-1)}] \quad (4.32)$$

Lastly, substituting (4.32) into (4.31) yields

$$I_{out} = I_L [N + \frac{A}{A-1} + log_A [\frac{g_m V_{in}(A-1)}{A^2 I_L}]] \quad (4.33)$$

which results in the logarithmic relationship between the input voltage and the output current. In this research, a wide dynamic range of 40 dB is targeted. Since the logarithmic amplifier's accuracy depends on the individual gain A_o of the limiting amplifier, a tradeoff is established between the individual limiting amplifier's small-signal gain and the required accuracy.

Design Guidelines The logarithmic amplifier design focuses on optimizing power consumption, sensitivity, dynamic range, and noise. The logarithmic amplifier total power consumption is given by

$$P_{total} = NI_{SS}V_{DD} \quad (4.34)$$

From (4.34), the total power consumption is directly proportional to the limiting amplifier tail current (I_{SS}) and the number of stages N. According to the expression ($DR = A^N$), for a fixed dynamic range, when the number of stages N is reduced, the limiters gain should increase. i.e., reducing N by a factor of 2 requires the gain to be raised by the power of 2 (A_V^2). Figure 48 shows that the limiters' gain decreases with increasing differential tail current (I_{SS}.). When the number of stages N is reduced for a fixed dynamic range, the power consumption will increase. Henceforth, the minimum possible N should be utilized to minimize power consumption, and Iss should be reduced. Nonetheless, subsection (2.4.4) established that the linear-in-decibel transfer

function's accuracy decreases with the limiters' increasing gain. Hence, a design trade-off between the number of stages N, differential tail current (I_{SS}), and the gain A^V must be established when designing the logarithmic amplifier for the targeted, dynamic range.

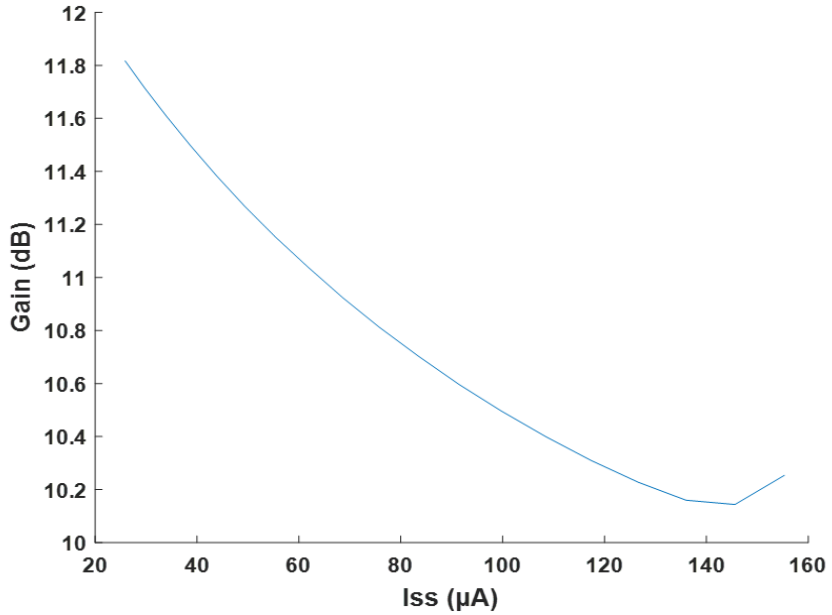


Figure 48: Iss vs. Gain of limiting amplifier.

Figure 49 shows a plot of the calculated theoretical design parameters in terms of I_{SS}, A_V, and input-referred noise for a target dynamic range of 40 dB

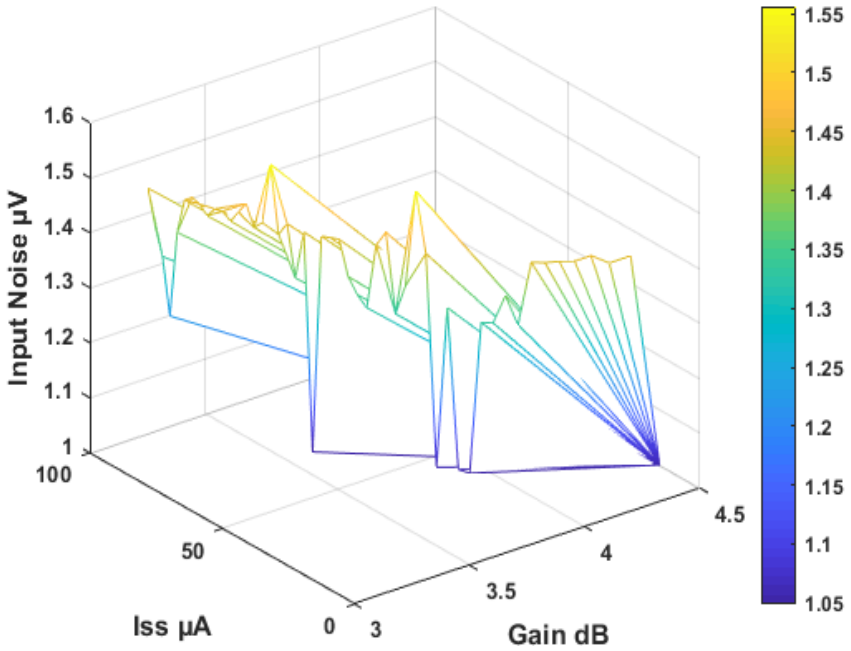


Figure 49: The limiting amplifier calculated design parameter.

It is important to note that the input noise considers only thermal noise sources. Figure 49 shows that for an input noise less than 1.5 μV, design conditions in the green region can be considered. For example, assuming gain (A_V) = 3.6 V/V, for a target dynamic range of 40 dB, N is equivalent to 5. Furthermore, to achieve an input noise less than 1.5 μV, an I_{SS} greater than 40 μA is required. Hence, considering the Input noise less than 1.5 μV and the target dynamic range of 40 dB, N = 5 is established as the optimum design condition for minimum power dissipation.

The specifications of the proposed logarithmic amplifier, which is designed to enhance its performance with regard to power consumption, dynamic range, and noise, are tabulated in Table 8.

Table 8: Logarithmic amplifier specifications

Parameters	**Value**
Dynamic Range (dB)	40
Number of stages	5
Error in the logarithmic characteristic (dB)	± 2
Operating bandwidth (Hz)	0.48k-0.8G
Low-level gain (dB)	11.5

Limiting Amplifier Circuit Configurations As mentioned in section 4.1, the logarithmic amplifier is employed to further amplify the RMS detector DC output voltage and enhance the linear range. The logarithmic amplifier consists of cascaded limiting amplifiers operating as voltage-limited gain cells with similar small signal gains. The gain cells generate both differential output current and voltage. The differential output voltage is passed to the succeeding limiting amplifier while the differential output currents are summed and applied to a resistor. Since the logarithmic amplifier's input is a DC voltage, an envelope detector and wide bandwidth are not required; thus, the design focus may be minimum power consumption. The limiting amplifier circuit configuration is illustrated in Figure 50.

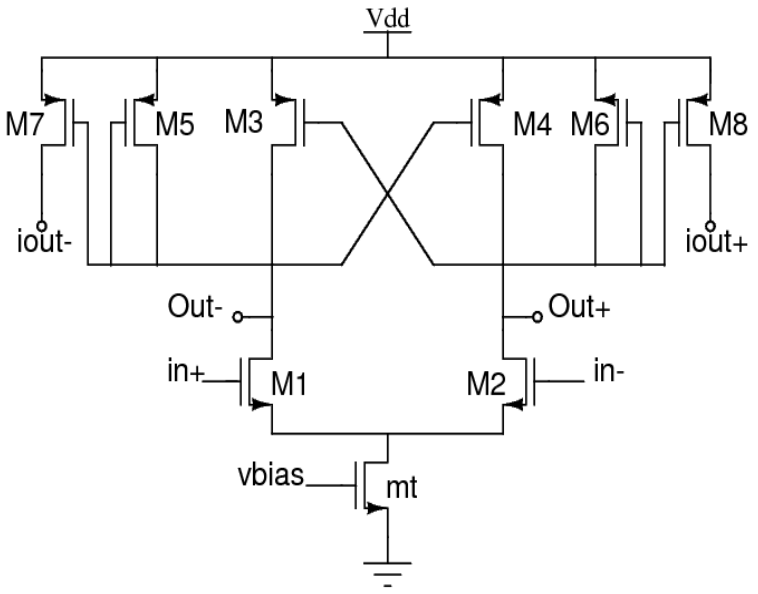


Figure 50: Limiting amplifier stage.

The complete logarithmic amplifier core utilizes a differential input circuit to prevent common-mode interference from other components on the chip (Muijs et al. 2013). The limiting amplifier is a fully differential cross-coupled operational transconductance amplifier with active loads. Cascode structure is usually employed to design limiting amplifiers because it increases the output impedance resulting in an enhanced gain. Furthermore, for same bias current and gain cascode structure offers higher bandwidth at the expense of greater output voltage swing. However, as large bandwidth is not a major requirement for limiting amplifier design in this study, slight emphasis was placed on cascode structure.

Since low power dissipation is crucial, differential topology is preferred due to its higher PSRR and CMRR in comparison to the single-ended topology (Banagozar & Yargholi 2019). Furthermore, the differential topology is less sensitive to temperature and supply voltage variations. In theory, a fully differential topology requires a common mode feedback circuit (CMFB) to monitor the common-mode output voltage (Ramos et al. 2011). However, the CMFB circuit increases the circuit overhead, thus the power consumption and chip area.

Moreover, the CMFB circuit is extremely sensitive to device mismatches and process variation, resulting to offset error. Hence, the diode-connected PMOS (M_5 and M_6) are designed as active loads. Since the diode-connected transistors lower the output nodes impedance, therefore the CMFB circuit is not necessary. The cross-coupled PMOS M_3 and M_4 are adopted since they

increase the voltage gain for a particular bias current. The differential output voltages are applied to NMOS transistors M_1 and M_2. The two-input transistors M_1 and M_2 widths must be relatively larger in comparison to their lengths to reduce flicker noise. The transistors M_7 and M_8 operate as a voltage to the current converter, generating the differential output currents summed to produce the linear-in-decibel output voltage. The maximum current generated by the transistors M_7 and M_8 determines the logarithmic slope. Thus, it is important to minimize the input offset voltage of the input transistors to maintain a fixed output current. The logarithmic amplifier is designed such that each limiting amplifier has a small signal gain between 10-13 dB as a trade-off between the number of stages and the logarithmic linear accuracy. It is important to note that the small-signal gain of the limiting amplifier is usually designed higher than 3 (9.5 dB) (Byun 2014; Chun-Pang & Hen-Wai 2005; Po-Chiun, Yi-Huei & Chorng-Kuang 2000; Yang & Mason 2008). Each of the cascaded limiting amplifiers is identical, and their voltage gain, neglecting channel length modulation, may be expressed as

$$A_v = \frac{gm_1}{gm_5 - gm_3} \tag{4.35}$$

The input transistors of the limiting amplifier are the dominant noise sources. The noises at the input of the limiting amplifier will be amplified by the gain over the whole bandwidth and then converted to DC voltage by the current to voltage converter transistors. Thus, thermal noise ($1/f$) becomes the logarithmic amplifier's core dominant source of noise. Therefore, a DC offset cancellation circuit in a feedback loop is required to minimize the thermal noise. Since minimum noise is achieved when the transconductance is maximized, the input transistor pairs M_1 and M_2 are biased in the weak inversion region (Zareie, Hosseinnejad & Azhari 2019). PMOS has a lower gm/id ratio than NMOS, generating greater thermal noise (Ayed, Ghariani & Samet 2005; Pinjare et al. 2018; Sabry, Omran & Dessouky 2018). As such, NMOS is preferred as an input pair for the proposed amplifier. The first stage contributes most of the overall noise; hence, it is crucial to enhance the first stage to minimize the noise. The tail transistor M_t should have a large W/L ratio and be biased in the strong inversion region. The tail current transistor M_t degenerates the input transistors' source with high impedance for the common-mode signal, thus reducing the gain of those signals. The input-referred flicker noise and the input-referred thermal noise of the limiting amplifier are given as

$$\overline{V_{ni,1/f}}^2 = 2\ X\ 4KT\gamma(\frac{1}{gm_1} + \frac{3gm_5}{2gm_1{}^2}) \quad (4.36)$$

$$V^2{}_{ni,th} = 2\ X\ 4KT\gamma(\frac{1}{gm_1} + \frac{3gm_5}{2gm_1{}^2}) \quad (4.37)$$

respectively, where K_p and K_n is the PMOS and NMOS transistor flicker noise coefficient and γ is the thermal noise coefficient. As mentioned prior, maximum transconductance is achieved by biasing the transistor in the weak inversion region. From equation 4.41, the limiter gain is determined by the transconductance of the MOS transistors. Furthermore, according to (4.36) and (4.37), both the input-referred thermal noise and the input-referred flicker noise are dependent on the transistor transconductance. Subsequently, to realize minimum noise and increased gain, the transconductance of the limiters should be maximized. Table 9 shows the dimensions of the transistors for the first stage.

Table 9: Transistors dimensions for the first stage

	W(µm)	**L(µm)**
M_1, M_2	2.00	0.18
M_3, M_4	0.65	0.18
M_5, M_6	0.80	0.18
M_7 , M_8	0.18	0.18
M_t	3.00	0.18

Bandwidth and Gain The number N of limiting amplifier stages employed for the cascaded logarithmic amplifier, and the circuit configuration of the limiting amplifier determines the dynamic range, linearity, bandwidth, and detection error of the RF power detector. The gain A_s and bandwidth f_s of a single limiting amplifier given A_t and f_t, the total gain, and bandwidth of the cascaded logarithmic amplifier can be expressed as (Kiela, Jurgo & Navickas 2013)

$$A_s = A_t{}^{1/N} \quad (4.38)$$

$$f_t = f_s\sqrt{2^{1/N} - 1}, \quad (4.39)$$

Furthermore, the total power consumption of a cascaded logarithmic amplifier can be calculated using the gain-bandwidth product (GBW) of a single limiting amplifier stage. The power dissipation of a single-stage limiting amplifier is directly proportional to the square of the GBW (Chokchalermwat & Supmonchai 2018). Therefore, the total power consumption of the cascaded logarithmic amplifier is given by

$$P_t \propto N \cdot (GBW_s)^2 = N \cdot \left(A_t \cdot \frac{1}{\sqrt{2^{1/N}}} f_s \right)^2 \tag{4.40}$$

Following equation (4.40), a trade-off between gain, bandwidth, and power consumption is a significant design consideration for the limiting amplifier. However, since wide bandwidth is not a major requirement in this research, the focus can be mainly on minimum power consumption and optimizing the gain. In addition to the power consumption, the number of cascaded limiting amplifiers establishes the log error of the transfer function. As mentioned in sub-section 2.4, the output voltage of the RF power detector employed using the successive detection method inherits log errors. The maximum log error in dB as compared to the ideal transfer function is given by (Byun 2014)

$$E_{max}(dB) = 10logA\left(\frac{log\frac{A-1}{lnA}}{logA} - \frac{1}{lnA} + \frac{1}{A-1}\right) \tag{4.41}$$

where A is the small-signal gain of the limiting amplifier. Cascaded limiting amplifiers are widely used in wireless communication and RF power detection. For example, for cascaded limiting amplifiers employed for GSM and wireless communication, a bandwidth of over 4 GHz is required to maintain wide power detection with excellent accuracy. Designing wide bandwidth limiting amplifiers in low voltage CMOS technologies has become challenging. However, since the input of the cascaded limiting amplifiers is a DC voltage, wide bandwidth is not necessary.

Frequency Response Figure 51 demonstrates the small-signal frequency response for the logarithmic amplifier and one limiting amplifier. The individual limiting amplifier and the logarithmic amplifier gain are 11.2 dB and 58.2 dB, respectively, while their bandwidths are 1.25 GHz and 430 MHz.

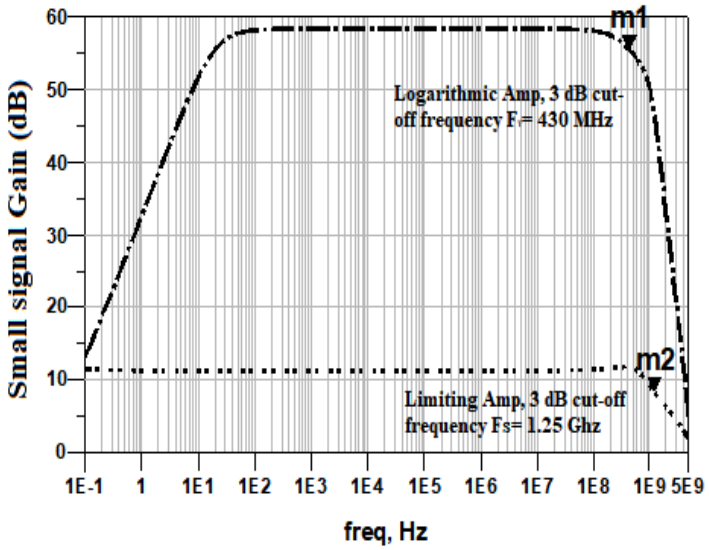


Figure 51: Frequency response of the logarithmic amplifier and one limiting amplifier stage

Gain Variation Over Temperature Constant gain over temperature is crucial for better accuracy and robustness to variations. Thus, it is necessary to optimize the design of the limiting amplifiers to reduce gain error over temperature (0 °C to 85 °C). Figure 52 shows the simulated small-signal gain of the limiting amplifier over temperature from 0.1 Hz to 5 GHz. The result shows that the gain error of the limiting amplifier over temperature is 0.8 dB.

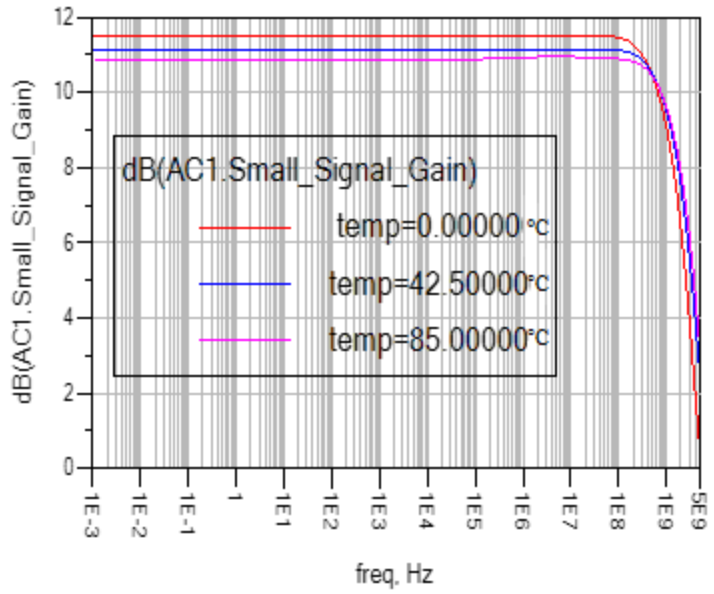


Figure 52: Limiting amplifier gain over temperature (0 °C to 85 °C)

Noise Analysis Figure 53 shows the simulated RMS output noise characteristics for the first stage of the limiting amplifier from 0.1 Hz to 5 GHz. As shown in Figure 53, the output noise

generated by the limiting amplifier is approximately 280 nV over a bandwidth of 5 MHz, which is still considered relatively low.

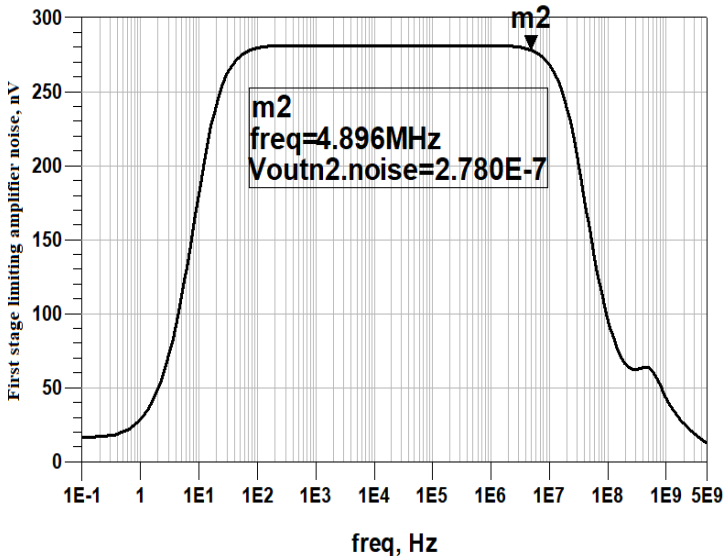


Figure 53: Simulated RMS output noise of the first stage limiting amplifier.

4.3.5. DC Offset Cancellation Circuit Configuration

Implementation When the differential inputs of the logarithmic amplifier are zero, the differential outputs ideally should be zero; however, an offset voltage is usually measured between the logarithmic amplifier outputs. This DC offset voltage resulting from device mismatch among the cascaded limiting amplifier stage may degrade the logarithmic amplifier input sensitivity and cause output saturation. DC offset at the output of the logarithmic amplifier can also decrease the dynamic range of the RF power detector. For this research, a removal mechanism that comprises a DC offset subtractor in a feedback loop and a first-order low-pass filter is employed. The feedback loop is preferred since the closed-loop gain reduces the limiter's input-referred offset voltage (Ramos et al. 2011). Furthermore, the feedback loop configuration offers less circuit overhead (Reimann & Rein 1987). The DC offset cancellation mechanism adopted in this research is shown in Figure 29. The DC offset subtractor realized using a cross-connected circuit architecture then subtracts the DC offset voltage (V_{OS+}, V_{OS-}) from the input signal (V_{in+}, V_{in-}). The output differential voltage V_{LA+} and V_{LA-} from Figure 29 are passed to the DC offset subtractor secondary input, and the negative feedback forces the logarithmic amplifier final stage differential output voltage to zero. Therefore, the offsets due to process and temperature variations are cancelled. The negative feedback structure generally decreases the

input offset voltage by a factor of the forward path cascaded voltage gain. The offset subtractor should have a voltage gain of 0 dB so that the signal is not degraded. Though the DC offset subtractor is in the signal path, the speed of the RF power detector will not degrade as the subtractor circuit introduces negligible parasitics (Huang 1998). All the transistors of the offset subtractor are biased in the strong inversion region. Figure 54 shows the circuit employed to design the DC offset subtractor, and its transistor dimensions are listed in Table 10.

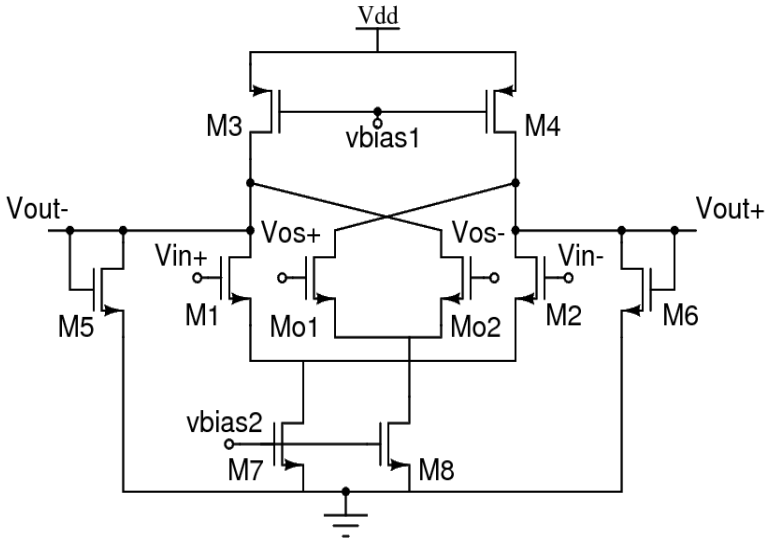


Figure 54: DC offset subtractor circuit

Table 10: Transistors dimension for the DC offset subtractor

	W(µm)	**L(µm)**
M1, M2	0.18	0.18
Mo1, Mo2	2.5	0.18
M3, M4	0.48	0.18
M5, M6	0.18	0.18
M7	0.9	0.18
M8	5	0.18

The low-pass filter extracts the DC output voltage, which is then subtracted by the input voltage. As shown in Figure 32, the low pass filter comprises capacitor C_f and pseudo resistors R_f. Since

the low pass filter must have a very low cut-off frequency, a large resistance and capacitance are required. MOSFETs pseudo resistors biased in the saturation region are adopted since they provide high resistance and smaller chip area compared to a resistor (Guglielmi et al. 2020; Huang et al. 2015; Pereira et al. 2017). The pseudo resistors behave as a Giga ohms resistor when the gate to source voltage is positive (Harrison & Charles 2003). Smaller values for the transistor size of the pseudo resistor and higher values for capacitor C_f decrease the 3-dB cut-off frequency of the low pass filter. The effective capacitance C_f and effective resistance R_f of the LPF are 15 pF and 482 G Ω.

Frequency Response The DC offset cancellation circuit in a negative feedback loop with the RF power detector core blocks is shown in Figure 55.

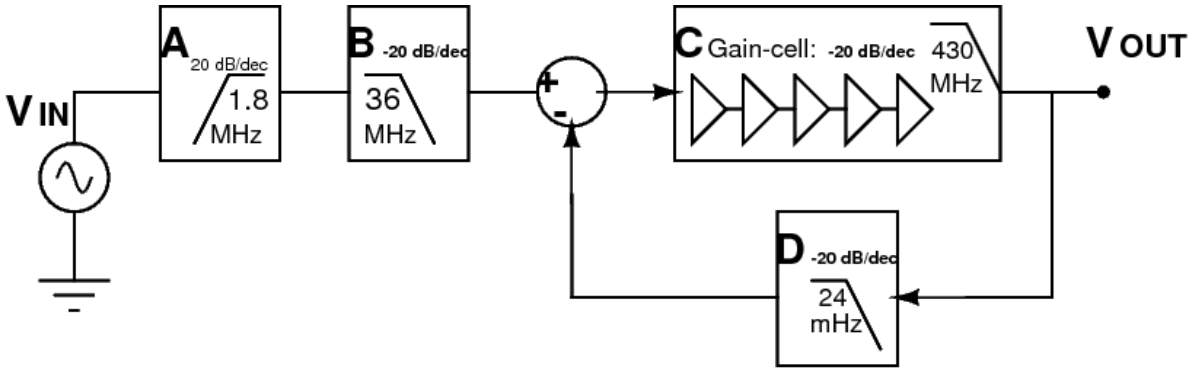


Figure 55: DC offset cancellation loop in the negative feedback loop block diagram

To analyse the transfer function of the RF power detector, let us define the frequency response of each blocks A, B, C, and D in the negative feedback configuration as

$$V_{OUT} = V_{IN}[A(s)B(s)C(s)] - V_{OUT}[C(s)D(s)]$$

$$= V_{IN}\frac{A(s)B(s)C(s)}{1+B(s)C(s)} \quad (4.42)$$

replacing A(s), B(s), C(s) and D(s) in equation (4.48)

$$A(s) = \frac{s\tau_A}{1+s\tau_A},$$

$$B(s) = \frac{1}{1+s\tau_B},$$

$$C(s) = \frac{1}{(1+s\tau_C)^5},$$

$$D(s) = \frac{1}{1+ s\tau_D},$$

$$\frac{V_{out}}{V_{in}} = \frac{s\tau_A(1 + s\tau_D)}{(1 + s\tau_A)(1 + s\tau_B)[(1+ s\tau_C)^5(1 + s\tau_D)+1]} \qquad (4.43)$$

Equation (4.43) establishes that the transfer function of the RF power detector is a band-pass response with multiple poles and two zeroes. Figure 56 compares the frequency response of the logarithmic amplifier with and without DC offset cancellation. As shown in Figure 56 (a), when offset compensation is provided, the frequency response of the logarithmic amplifier has a band-pass characteristic. The cascaded limiting amplifier frequency response has a high-pass cut-off frequency and low-pass cut-off frequency of 18.75 Hz and 430 MHz with offset compensation. Therefore, the transfer of signals with frequencies less than 18.75 Hz is flat.

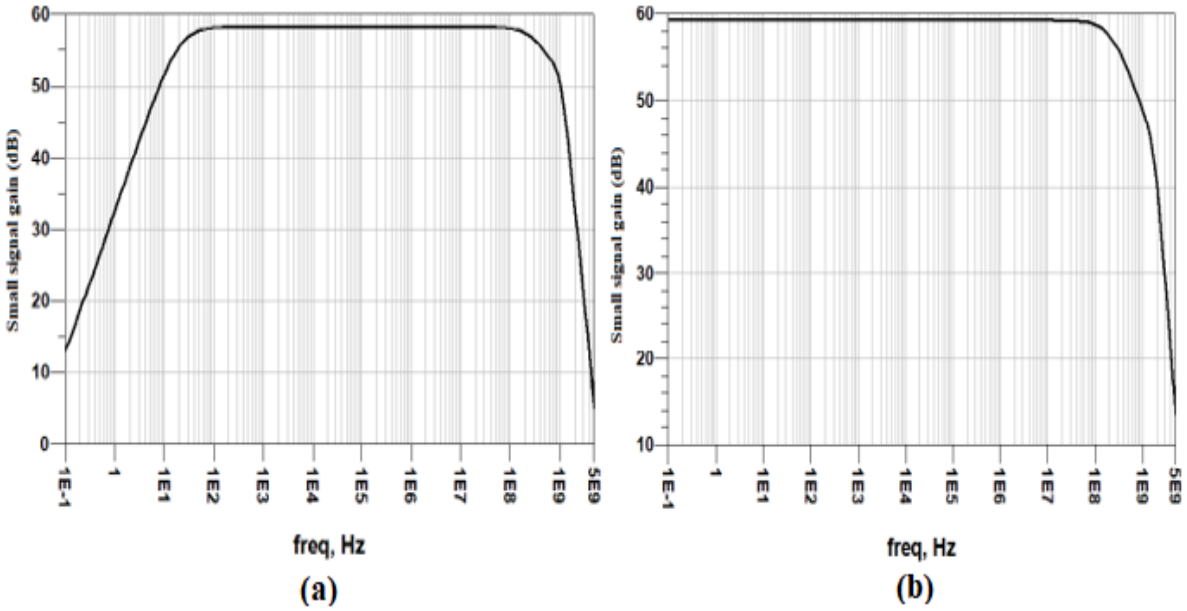


Figure 56: frequency response of the cascaded limiting amplifier (a) with DC offset cancellation circuit (b) without the DC offset cancellation circuit

The AC simulation of the small-signal gain of the RF power detector shown in Figure 56 (a) validates (4.43). A bandpass response is preferred so that low frequencies noise signals at the input transistors are not transmitted. The cascaded limiting amplifiers generate constant gain over the bandwidth of operation down to DC. The DC offset cancellation circuit avoids saturation of the logarithmic amplifier output swing caused by unwanted low-frequency signals. A DC offset cancellation circuit employed in a feedback loop will reduce the low-frequency gain giving the logarithmic amplifier band-pass transfer characteristic. Figure 57 shows the frequency

response of the low pass filter, and as it can be seen, the cut-off frequency of the low pass filter is approximately 24 mHz.

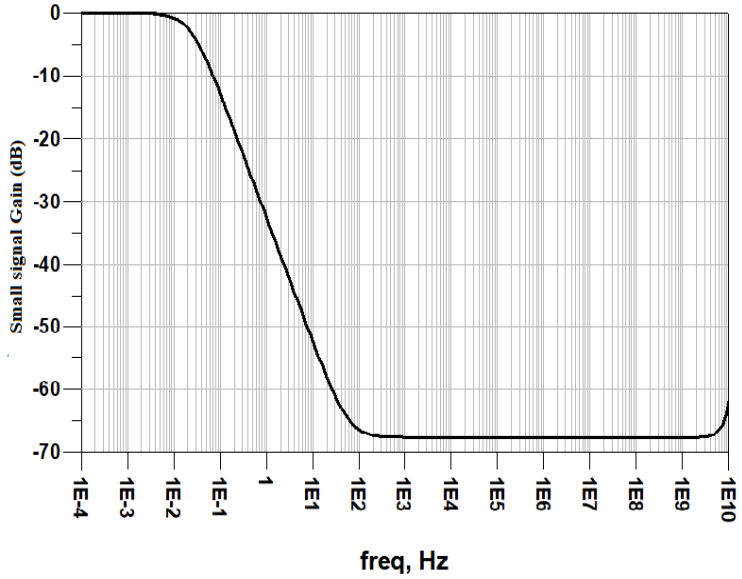


Figure 57: Frequency response of the low pass filter

Figure 58 shows the frequency response of the DC offset subtractor. As shown in Figure 58, a small signal gain of 0 dB is simulated, which is crucial to avoid signal deterioration. The glitch in the frequency response of the DC offset subtractor at higher frequencies is due to a delay that occurs between input signal and the DC offset voltage causing a small error in the subtraction.

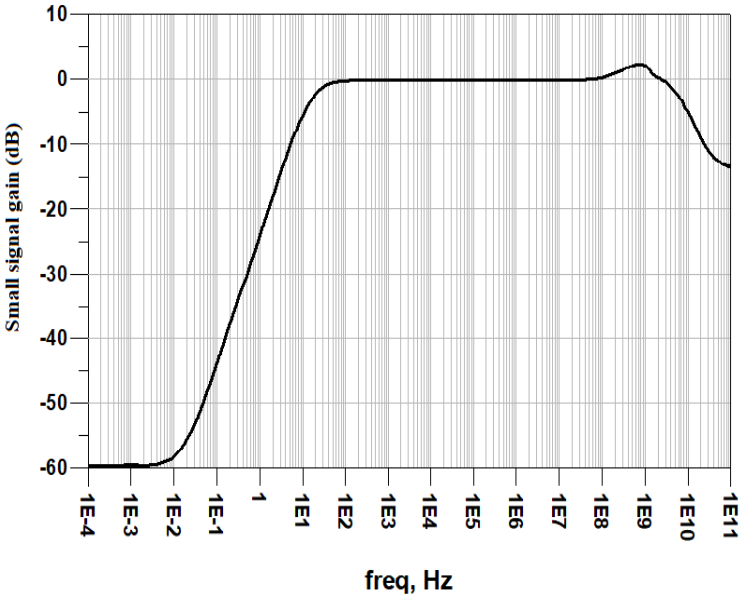


Figure 58: Frequency response of the DC offset subtractor

4.3.6. Bandgap Voltage Reference

Implementation In analogue, digital, and RF circuits, a voltage reference independent of process, voltage, and temperature variations is crucial (Khan 2018; Mohammed et al. 2016). The stability of the voltage reference establishes the system's accuracy and performance functionality. The voltage reference circuit architecture may be categorized into three main functions: generation of a complementary to absolute temperature (CTAT) voltage, generation of a proportional to absolute temperature (PTAT) voltage, and biasing. A simple Bandgap Reference circuit (BGR) generates a voltage resistant to voltage drift over temperature and power supply variations is employed in this research. Figure 59 shows the circuit configuration of the BGR adapted from (Ka Nang & Mok 2002). In CMOS technology, bandgap reference is implemented using a parasitic vertical BJT formed between the n-well and p+ implant (Bakker & Huijsing 1996). The BGR composes a start-up circuit, a PTAT current generator, a CTAT current generator, and a self-biased differential amplifier. The self-biased amplifier forces the same current through both sides of the bandgap reference. One significant advantage of this topology is that smaller VDD can be used without affecting the bandgap reference voltage.

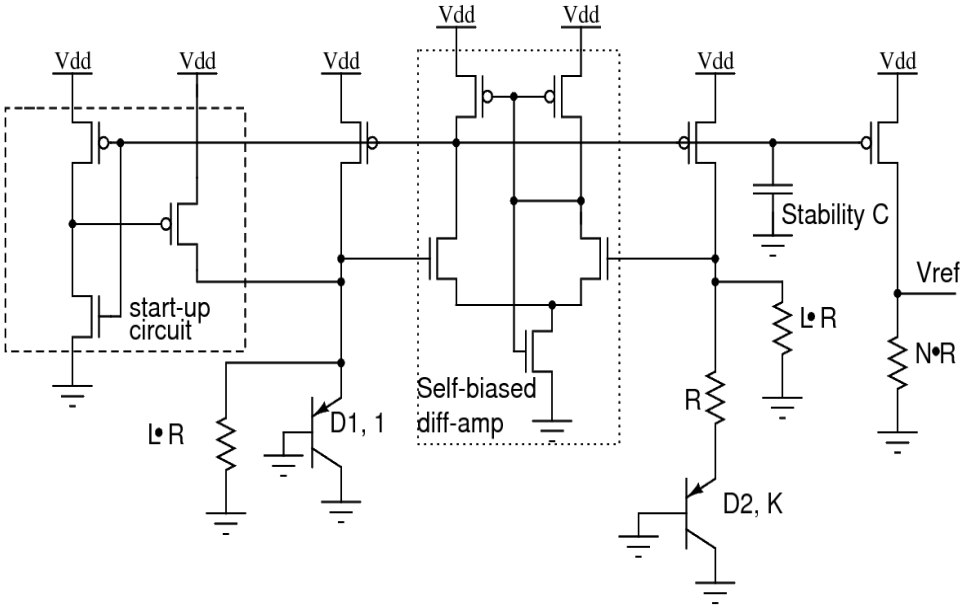


Figure 59: BGR circuit configuration

From Figure 59, the resistor, R, diodes D1, and D2 generate a PTAT current. Considering the current mirror configuration, the voltage across the D2 and R must be equal to the voltage across D1.

$$V_{D1} = V_{D2} + I_{D2}R \quad (4.44)$$

Equation (4.44) indicates that the voltage drop across R represents the voltage difference of the diodes. As such, for a current to flow in the reference, D1 must be smaller than D2. The current across D1 and D2 is given by

$$I_{D1} = I_S e^{V_{D1}/nV_T} \rightarrow V_{D1} = nV_T \cdot ln\frac{I_{D1}}{I_S} \quad (4.45)$$

$$I_{D2} = K \cdot I_S e^{V_{D2}/nV_T} \rightarrow V_{D2} = nV_T \cdot ln\frac{I_{D2}}{K \cdot I_S} \quad (4.46)$$

where V_T is the thermal voltage, n, the current gain factor, K the ratio of the junction of the two diodes, and I_S, the reverse saturation diode current. In this project, K = 8 was utilized. Since we have established that because of the current mirror structure, $I_{D1} = I_{D2} = I$, then we write

$$I_{PTAT} = \frac{nk \cdot lnK}{qR} \cdot T \quad (4.47)$$

where q is the electron charge and k the Boltzmann constant. According to equation (4.47), the current is proportional to absolute temperature (PTAT). To obtain a CTAT voltage, let us consider the L.R resistors, as shown in Figure 56. The CTAT is generated across the base-emitter (V_{BE}) of the BJT. An increasing temperature will cause a decrease in the diode voltage, resulting in a CTAT current across the L.R resistors. The CTAT current across the L.R resistor may be expressed as

$$I_{CTAT} = \frac{V_{D1}}{L \cdot R} \quad (4.48)$$

Therefore, the bandgap voltage reference is generated through the N.R resistors by summing the PTAT and CTAT references. When the bandgap reference is designed accurately, the temperature coefficient (TC) can be negligible. The reference voltage through the N.R resistance is then given by

$$V_{ref} = nV_T \cdot N \cdot lnK + \frac{N}{L} \cdot V_{D1} \quad (4.49)$$

The temperature behaviour of the BGR is

$$\frac{\partial V_{ref}}{\partial T} = n \cdot N \cdot lnK \cdot \frac{\partial V_T}{\partial T} + \frac{N}{L} \cdot \frac{\partial V_{D1}}{\partial T} \quad (4.50)$$

The BGR shown in Figure 56 is a self-bias circuit, meaning it is supply independent. One primary concern of such circuit configuration is that a degenerated bias condition can occur. This condition arises when current is not flowing through the branches causing the circuit to remain in non-operating condition indefinitely (Caylor 2007). Therefore, a start-up circuit is required to inject current into the circuit when the BGR is powered on to prevent a degenerated bias condition. The start-up circuit should not affect the normal operation of the BGR or consume too much power. The stability capacitor C helps to maintain the reference voltage stable. A larger value of C enhances the reference voltage stability at the expense of a longer start-up time (Ka Nang & Mok 2002).

4.4. Conclusion

This chapter covers the design and analysis of the linear-in-decibel RF power detector using a 180 nm CMOS technology. The circuit configuration of the RF power detector, which composes an RMS power detector unit, a wideband input matching, a cascaded logarithmic amplifier, and a DC offset cancellation circuit, was depicted in detail. A stepwise mathematical analysis is presented on how power detection and linear-in-decibel output are realized. MOSFET operation in the different inversion regions and the second-order effects, such as the short-channels effect, is also analysed. Justification for the RF power detector circuit configurations and the design guidelines are established. Simulation of the various components is also carried out to validate the design and optimize performances in the dynamic range, sensitivity, and power consumption. As a trade-off between these critical parameters, a current source-load, a five-stage logarithmic amplifier, and a DC offset cancellation in a feedback look were employed to realize design specifications.

Chapter 5

Results and Discussions

This chapter presents the results and discussions of the proposed linear-in-decibel RF power detector depicted in chapter four. The performance of the RF power detector is verified through simulations based on the specifications set in subsection 3.2.7 The critical parameters such as dynamic range, operation frequency, and sensitivity are verified. The simulations were accomplished with Keysight ADS using the 180 nm CMOS technology process transistor parameters (BSIM3V1). The performance results of each block that compose the RF power detector are investigated and discussed thoroughly. All simulations were carried out at room temperature, and a nominal voltage of 1.8 V was utilized. Performance comparison of the proposed RF power detector and recent power detector found in literature is provided at the end of this chapter.

5.1. Bandgap Voltage Reference

The bandgap voltage reference shown in Figure 59 was successfully simulated in Keysight ADS using 180 nm CMOS technology process parameters.

DC Analysis DC simulation of the reference voltage for the temperature range of -40 °C to 85 °C was carried out to verify the bandgap reference voltage's performance.

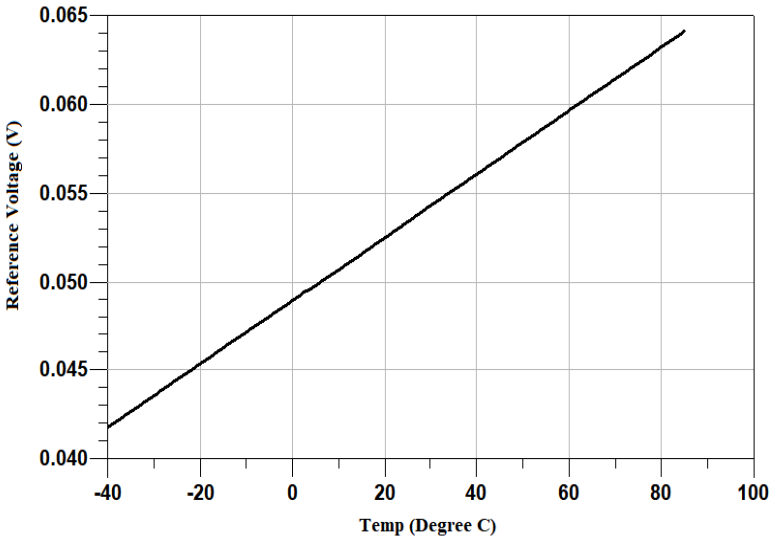


Figure 60: PTAT Voltage Reference

Figure 60 shows the PTAT reference voltage across resistor R, while Figure 61 shows the CTAT voltage.

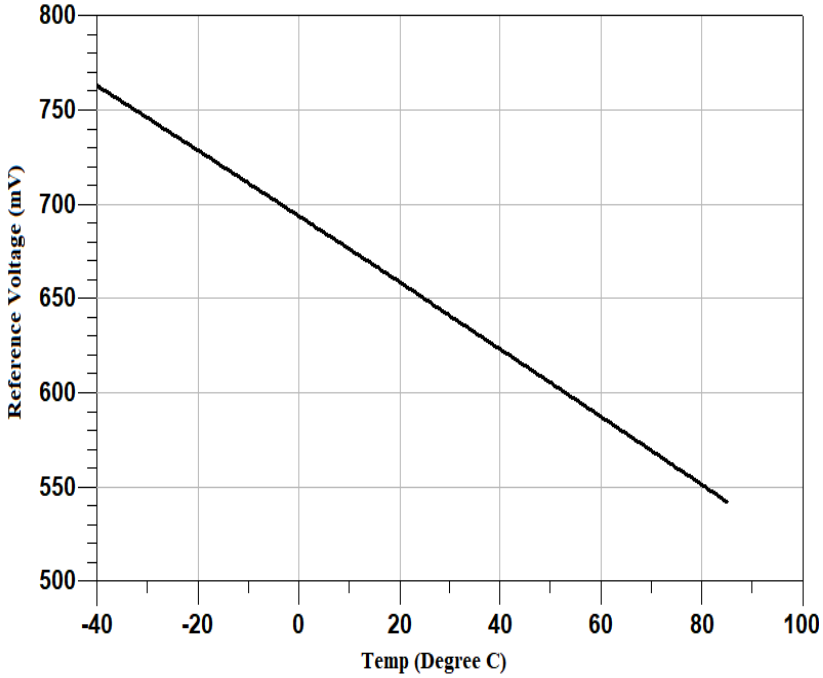


Figure 61: CTAT Voltage Reference

As shown in Figure 60, the reference voltage increases with increasing temperature (proportional to absolute temperature). In contrast, in Figure 60, the reference voltage decreases with increasing temperature (complementary to absolute temperature). From Figure 61 simulation data, we can approximate the change in reference voltage with temperature as

$$\frac{dV_D}{dT} = -1.75\, mV/°\text{C} \qquad (5.1)$$

It is important to note that this number is highly dependent on the DC current across the diode. Figure 62 shows the bandgap reference voltage across the N.R resistor, which results from the addition of the PTAT and CTAT reference voltages. As shown in Figure 62, a mean voltage of 800 mV is simulated with a variation of ±5 mV when the temperature is changed from -40 °C to 85 °C. The Temperature Coefficient (TC) of the BGR over the whole temperature range (-40 °C to 85 °C) is 50 ppm/°C for a VDD of 1.8 V. Figure 63 shows the reference voltage as the supply voltage is varied from 0 to 2.6 V. The bandgap reference generates a constant reference voltage of 800 mV over a supply voltage range from 1.8 to 2.6 V at room temperature.

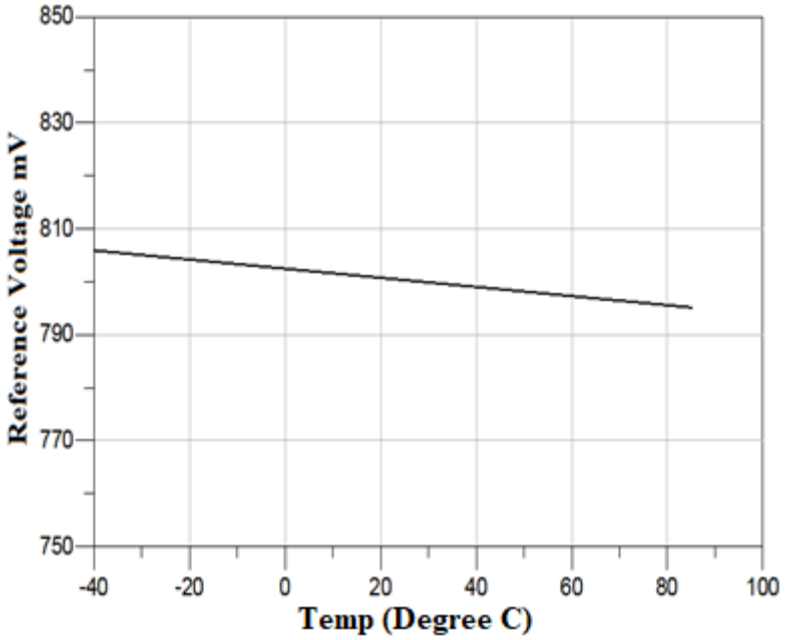


Figure 62: Temperature dependence of the Bandgap reference voltage

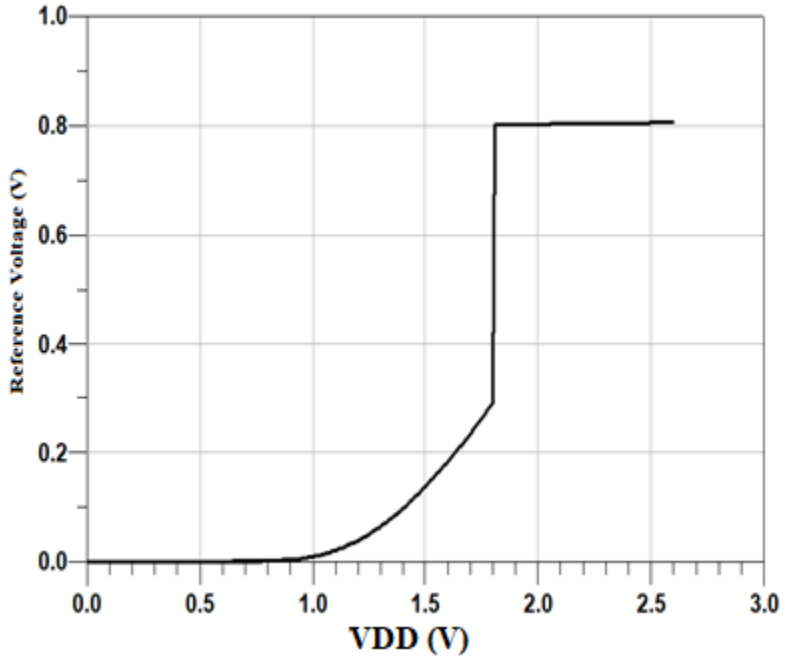


Figure 63: Simulated reference Voltage as a function of power supply at room temperature

Transient Response Figure 64 (a) shows the reference voltage transient response of the self-biased BGR without the start-up circuit, while Figure 64 (b) shows the transient response when the start-up circuit is connected to the self-biased BGR. Transient simulations were run with

VDD set as a pulse voltage whereby V_low = 0 V and V_high = 1.8 V. The delay between V_low and V_high was set to 1 µS and the rise and fall time was 1 nS for a period of 100 µS. As shown in Figure 61 (a), without the start-up circuit, the reference voltage of the BGR is 0 V. As mentioned in sub-section 4.1.5, this is because there is no current flowing through the branches resulting in degenerated bias condition. From Figure 61 (b), when the self-biased is connected to a start-up circuit, even for the condition where V_low = 0 V, the reference voltage of 0.8 V is maintained. Figure 62 (b) shows that the reference voltage of 0.8 V is achieved after only 15 µS. The start-up time can be decreased by reducing the stability capacitance C at the expense of the reference voltage stability. When designing self-biasing references, start-up is a key feature.

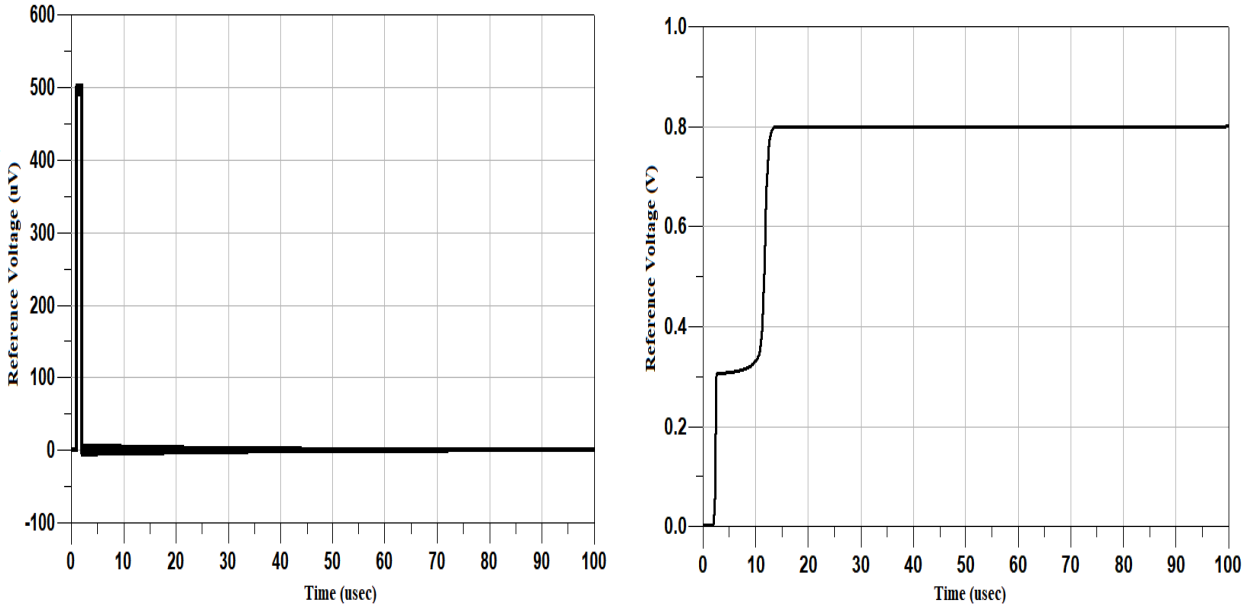


Figure 64: (a) Reference voltage without start-up (b) Reference Voltage with start-up circuit

Power Supply Rejection Ratio (PSRR) The PSRR of the bandgap voltage reference circuit is also an important performance parameter. The PSRR of the bandgap voltage reference circuit indicates the tolerance of the reference voltage to power supply noise over a specified frequency range. Therefore, the PSRR is utilized to compute the voltage reference capability to reject unwanted signals and noise while tied to the power supply rails at a specified frequency. Since the BGR is a DC-based circuit that does not involve any signal propagation from an input to an output, the PSRR of the reference voltage is usually derived at low frequencies. As shown in Figure 65, a PSRR of around -52 dB was simulated from 1 Hz to 1 kHz for the BGR.

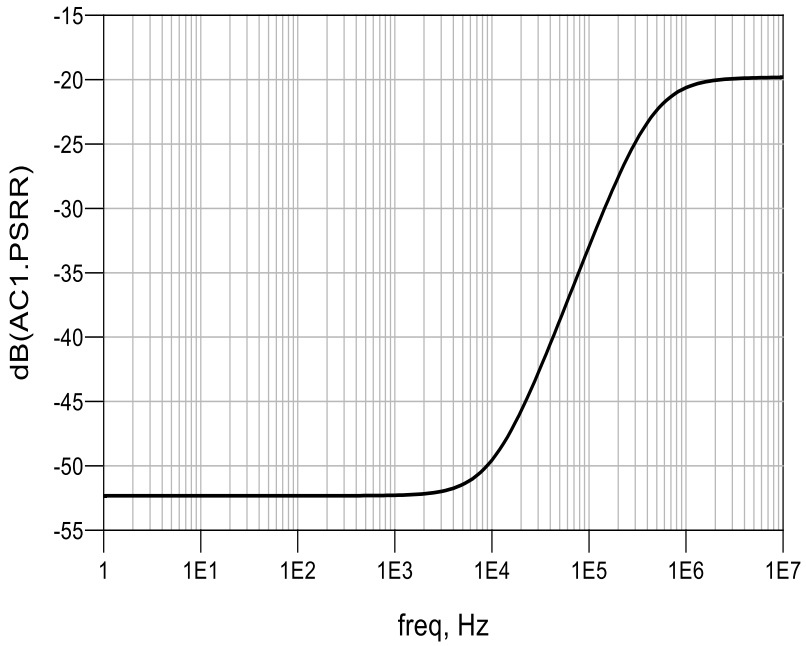


Figure 65: BGR PSRR

Monte Carlo Analysis A series of simulations were run to determine the effects of parameter mismatch and process variations on the reference voltage of the BGR. Figure 66 illustrates the Monte Carlo (MC) histogram of the reference voltage at room temperature (27 °C) across 500 runs. The mean and standard deviation of the V_{ref} parameter is 0.802 V and 1.96 V, respectively.

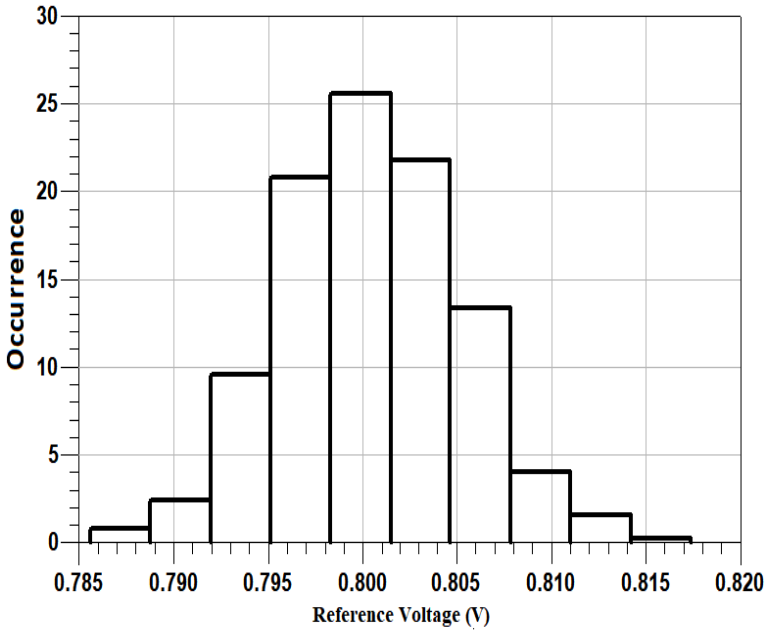
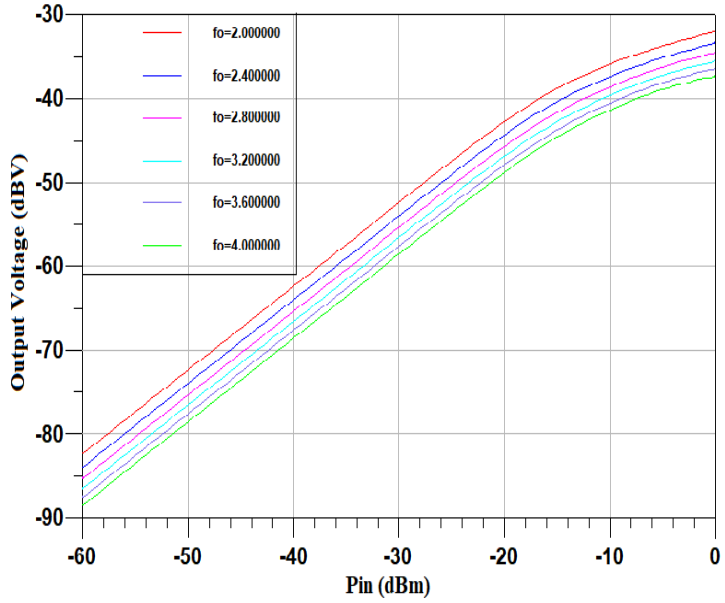


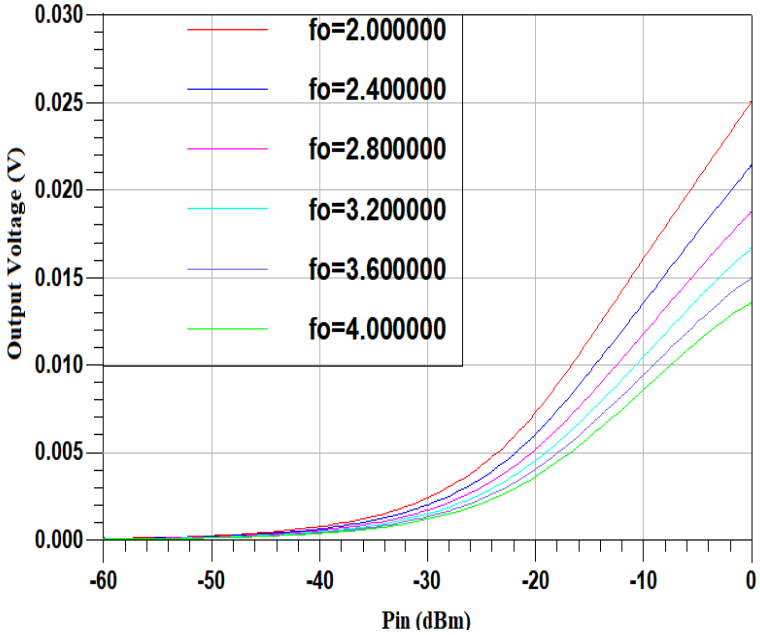
Figure 66: Monte Carlo (MC) histogram of V_{ref} at 27 °C

5.2. The RMS Detector

Harmonic Balance Analysis The current-source-load RMS power detector response preceding the logarithmic amplifier was assessed at different frequencies. Figures 67 (a) and 67 (b) show the simulation results of the RMS power detector both in the logarithmic and linear format in a range of 2 GHz (from 2 GHz to 4 GHz).



(a) Logarithmic

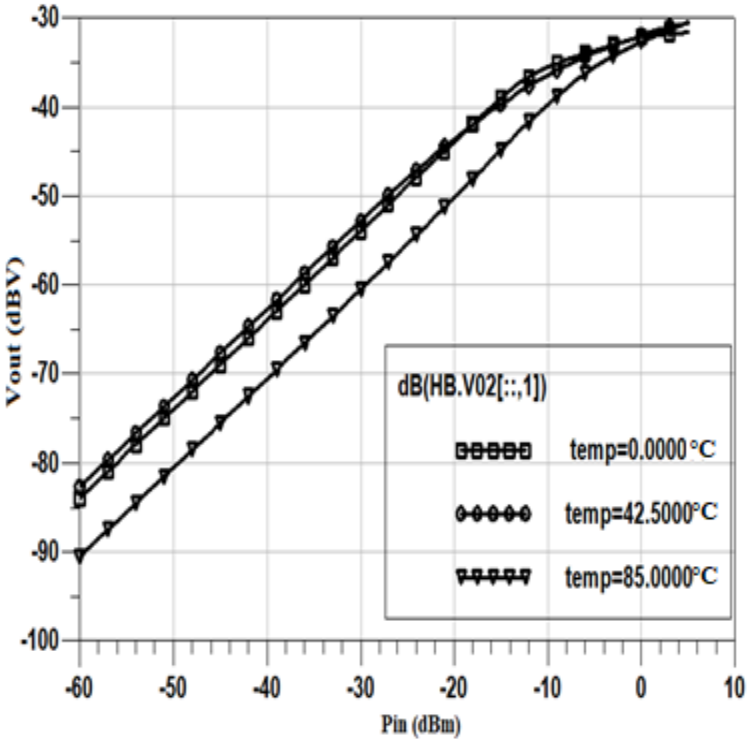


(b) Linear

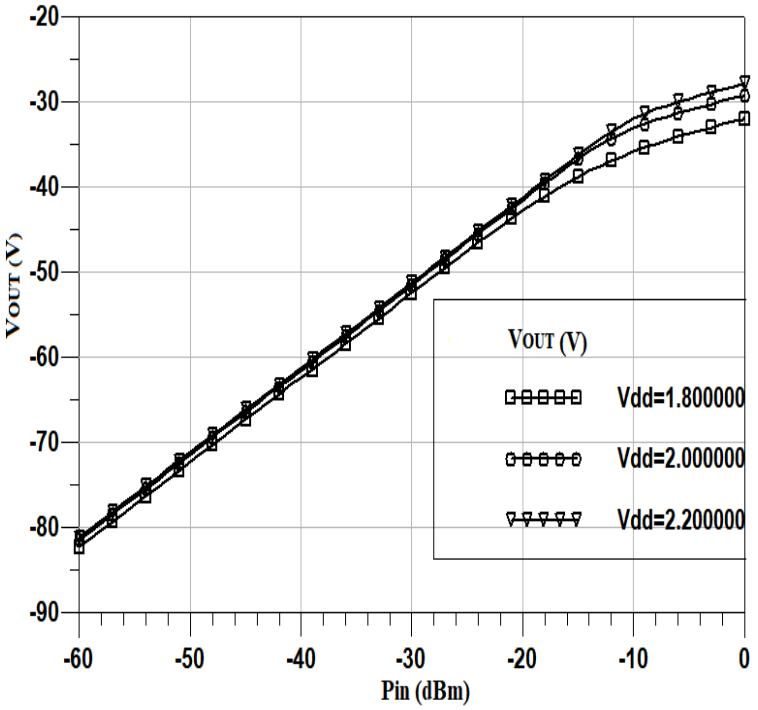
Figure 67: RMS power detector differential output voltage

As shown in Figure 67 (b), when the RMS power detector is biased in the strong inversion region, a square-law relationship is established between the input signal and the output voltage until it goes into the linear region. The RMS power detector utilized this square-law relationship to perform power detection as found in equation (4.13). When the RMS power detector goes out of the strong inversion region, the linear region begins, which, as shown in Figure 67 (b), starts from -17 dBm. Referring to the RMS power detector differential output in the logarithmic format, as shown in Figure 67 (a), the RMS power detector goes into saturating state when the linear region begins.

Figure 68 (a) and 68 (b) show the transfer function of the RMS power detector under temperature and supply voltage variations, respectively. It is to validate the operation of the circuit under those conditions. Since the proposed power detector aims at wireless applications in the agriculture sector, a temperature range of 0 °C to 85 °C was chosen for this research. The simulation results demonstrate that the power detector can work appropriately under temperature and supply voltage variations.



(a)



(b)

Figure 68: Input-output characteristics under (a) temperature and (b) supply voltage variations

Frequency Response Figure 69 shows the frequency response of the RMS power detector. A small-signal gain of 23 dB with a 3 dB cut-off frequency of 36.24 MHz is simulated. The high small-signal gain and the limited bandwidth are due to the cascode circuit configuration of the RMS power detector. A trade-off between the small-signal gain and the bandwidth was established to enhance the performance of the RF power detector. This is because the output voltage of the power detector depends on the gain. When the power detector has a low gain, larger input signals can be detected because sensitivity decreases. On the contrary, sensitivity is enhanced when the power detector has a high gain; thus, weaker input signals can be detected. As stated in sub-section 2.2.1, consistent response over frequency depends on the impedance input matching and the gain variation against frequency. Referring to Figure 69, which shows a limited bandwidth of 36.24 MHz for the RMS detector, and Figure 67 (a), which shows a decrease in the differential output voltage from 2 GHz to 4 GHz, it can be concluded that the inconsistency of the differential output voltage over frequency is due to the declining gain of the RMS power from 2 GHz to 4 GHz.

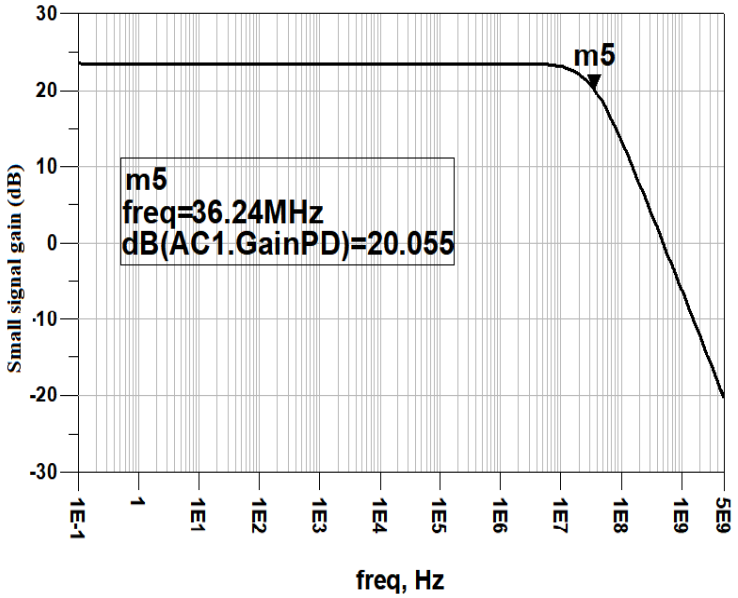


Figure 69: Frequency response of the RMS power detector

Transient Response Figure 70 shows the transient response of the RMS power detector when the input power is swept from -60 dBm to 0 dBm at 2 GHz. As shown in Figure 70, the transient output voltage increases with increasing input power. A settling time of approximately 20 nS is simulated for the RMS power detector unit. The decoupling capacitor influences the settling time between the input signal and the RMS power detector to reduce noise.

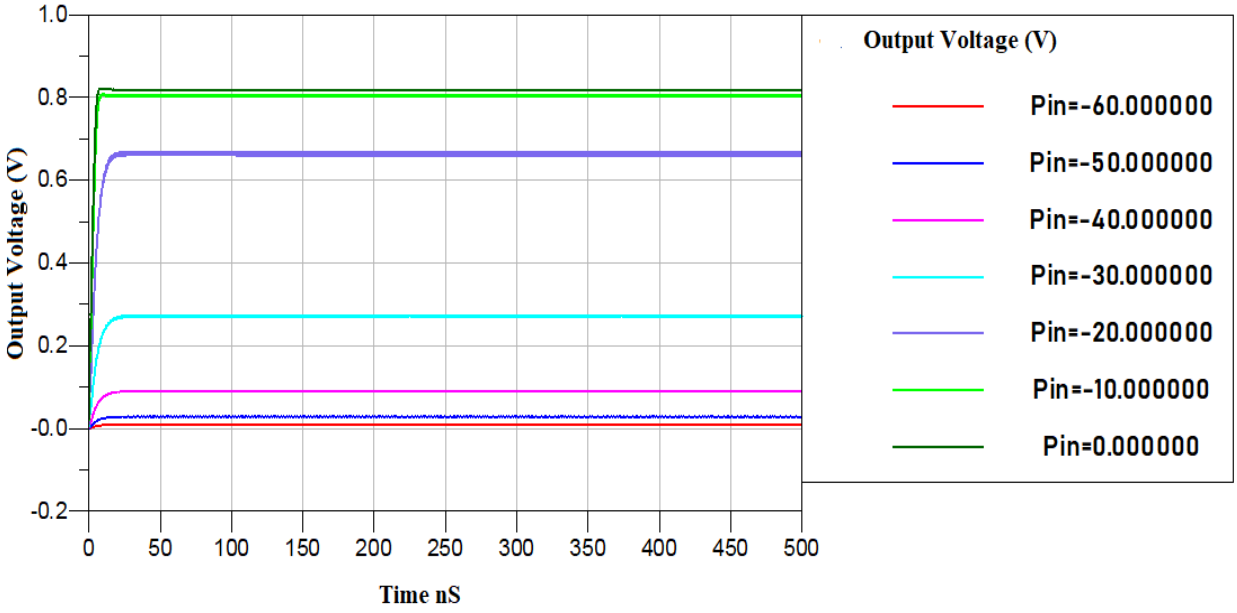


Figure 70: Transient response of the RMS power detector when the input power is swept from -60 dBm to 0 dBm at 2 GHz

5.3. The RF Power Detector

Harmonic Balance Analysis As mentioned, prior, the differential current generated by the limiting amplifiers are summed together and applied to a resistor Rs to produce the RF power detector linear-in-decibel output voltage. Figure 71 shows the RF power detector simulated linear-in-decibel output voltage for different resistance Rs at 2 GHz. As shown in Figure 71, the value of Resistor Rs influences the slope of the linear-in-decibel output voltage. In this research, a resistance Rs of 117.5 kΩ was utilized to sum the cascaded limiting amplifiers' differential output currents, thereby generating the linear-in-decibel output. The calculated slope of the RF power detector transfer function when Rs is 117.5 kΩ at 2 GHz was 13.2 mV/dB. It is important to note that a filtering capacitor is usually added at the output of the RF power detector to extract the DC output. However, since the input of the cascaded limiting amplifier was a DC voltage, a filtering capacitor is not required at the output of the RF power detector.

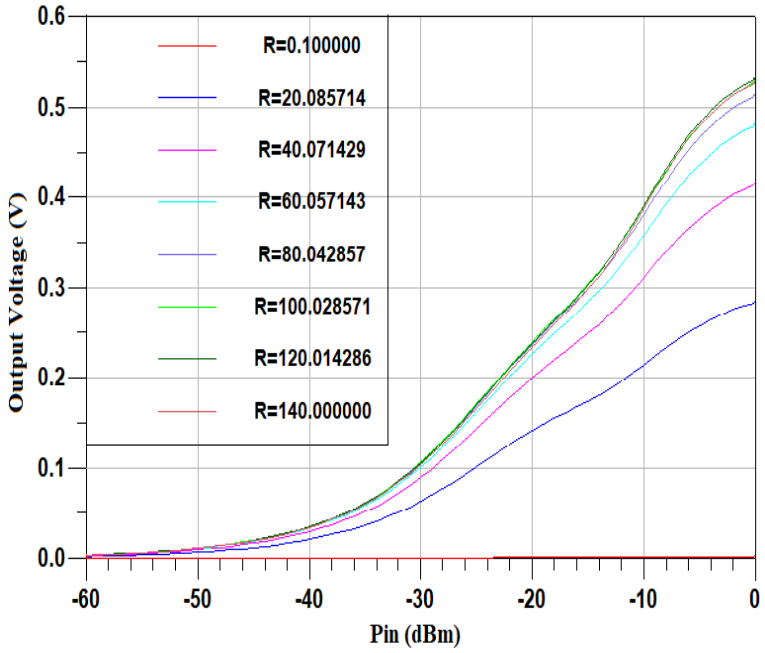


Figure 71: Output Voltage of the RF power detector at different resistance Rs

To validate the operation of the RF power detector, the input signal was swept from -60 dBm to 0 dBm at different frequencies. Figure 70 demonstrates the simulated input-output characteristics of the RF power detector from 2 GHz to 4 GHz. With an input range of -60 dBm to 0 dBm, the linear-in decibel output voltage ranges between 0.05 V to 0.54 V. A minimum detectable input signal of -55 dBm at 2 GHz and -38 dBm at 4 GHz was simulated as shown in Figure 72. Figure

73 shows the log error of the RF power detector output voltage when referring to the ideal logarithmic transfer function for all the frequencies in Figure 71.

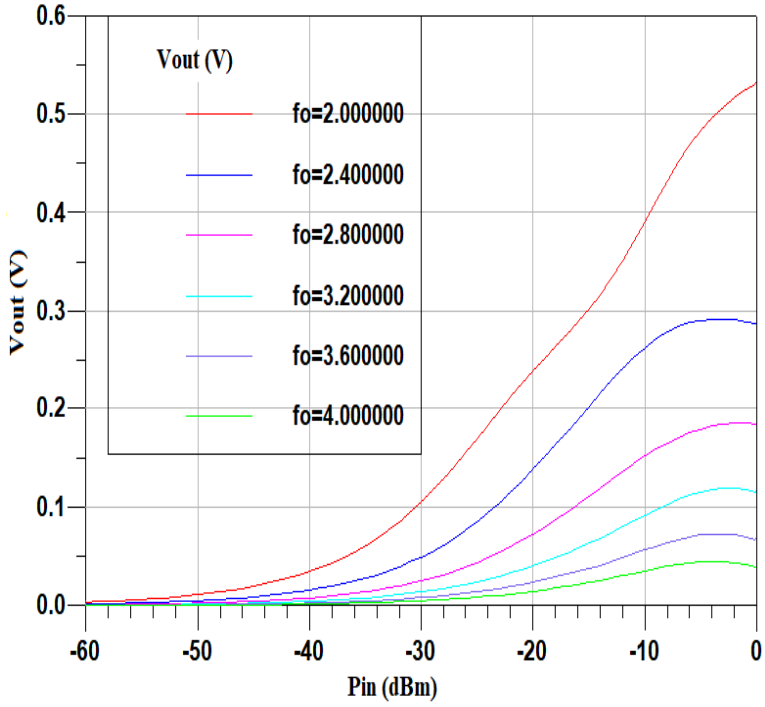


Figure 72: Input-output characteristics of RF power detector

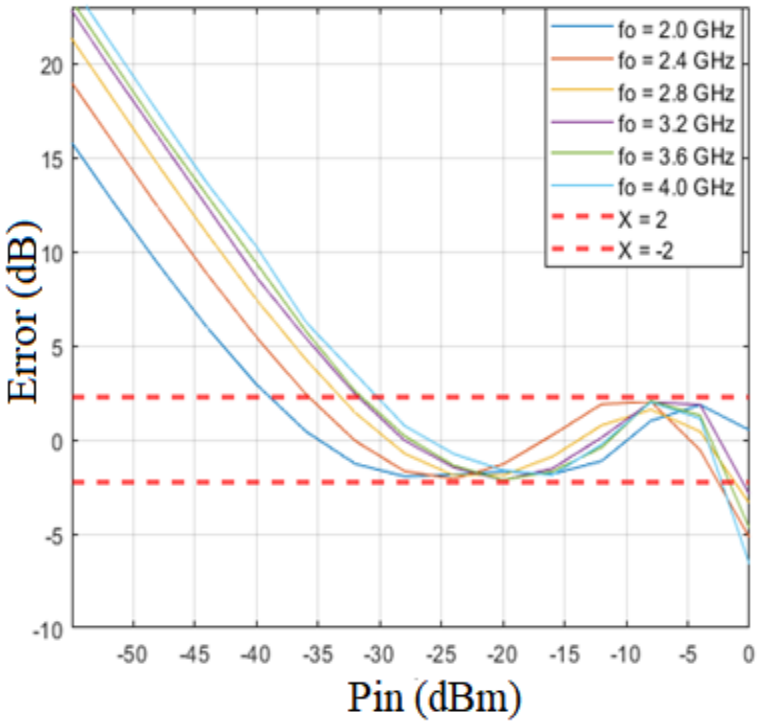


Figure 73: Simulated log errors (dB) versus input power (dBm)

The simulated dynamic range is 40 dB at 2 GHz and 30 dB at 4 GHz, with the log error less than ± 2 dB. The decrease in output voltage as the operating frequency increases from 2 GHz to 4 GHz is due to the declining gain of the RMS power detector preceding the logarithmic amplifier. The simulation results imply that the power detector could detect input power levels for frequencies up to 4 GHz.

Figure 74 shows the simulated output voltage of the RF power detector with or without the preceding current-source-load RMS detector at 2 GHz. As shown in Figure 74, the addition of the RMS detector shifts the power detector detection range, thus improving the sensitivity by 20 dB. Similar observations were seen in (Yingbo et al. 2012), where the RF power detector sensitivity was improved by 24 dB when an LNA preceded the RF power detector. In addition, it is important to note that the addition of the RMS detector does not affect the transfer function slope and the detection range of the power detector.

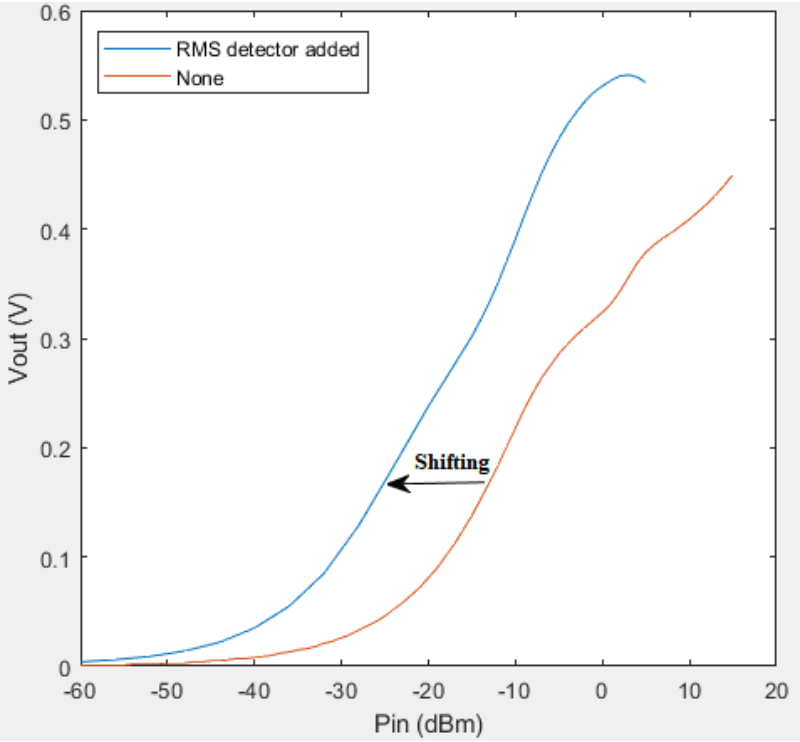


Figure 74: Output voltage with or without the preceding RMS power detector at 2 GHz

Noise Analysis Figure 75 shows the simulated Noise Figure (NF) of the RF power detector over the frequency range of 2 GHz to 4 GHz. The simulated noise Figure demonstrates good noise performance of less than 10 dB over the frequency range of 2 GHz to 4 GHz.

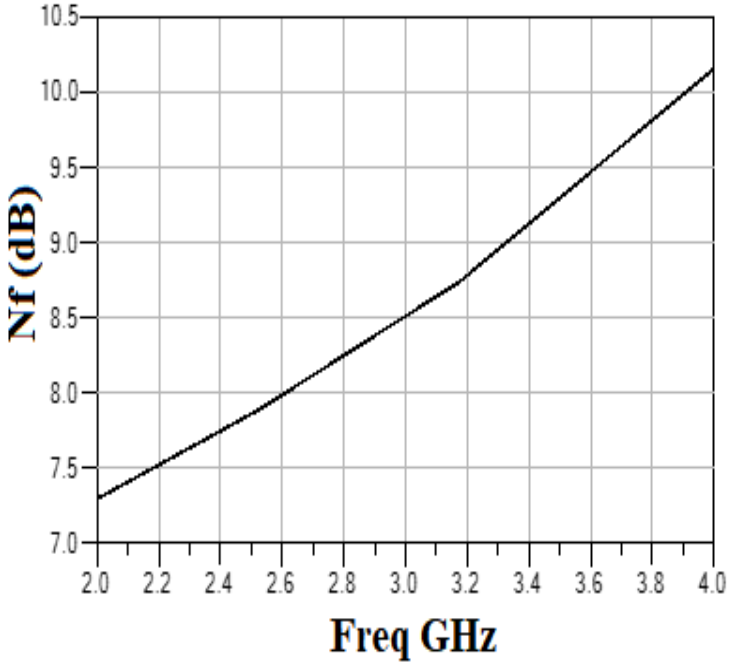


Figure 75: Noise Figure of the RF power detector

Figure 76 shows the simulated RMS noise characteristic at the output of the RF power detector from 0.1 Hz to 5 GHz. As shown in Figure 76, the output noise generated by the RF power detector is approximately 5 µV over a bandwidth of 70 MHz, which is still considerably low.

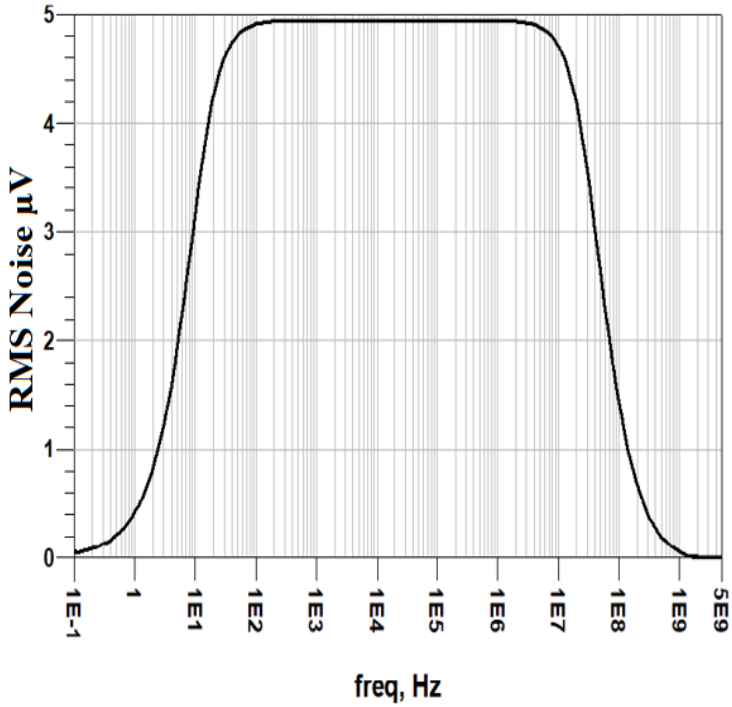
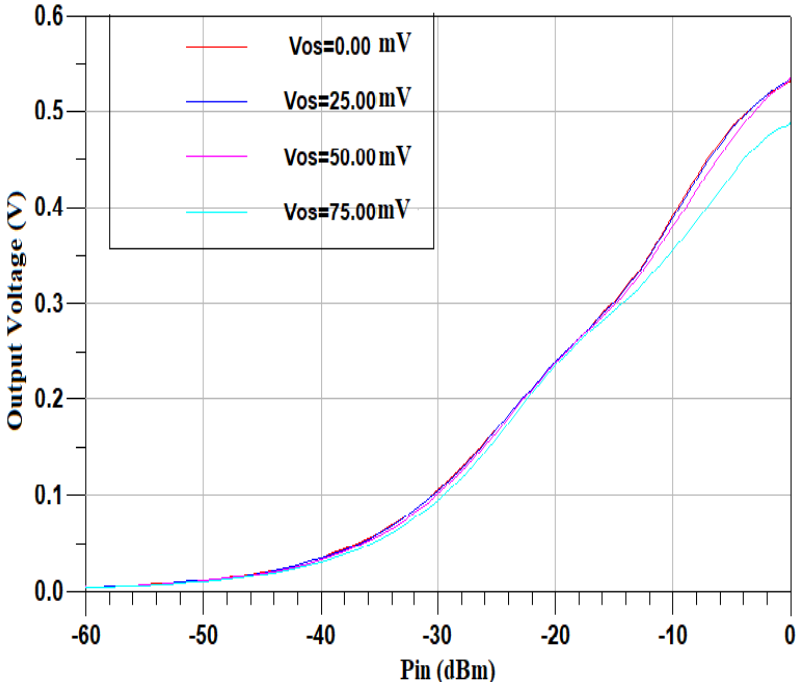
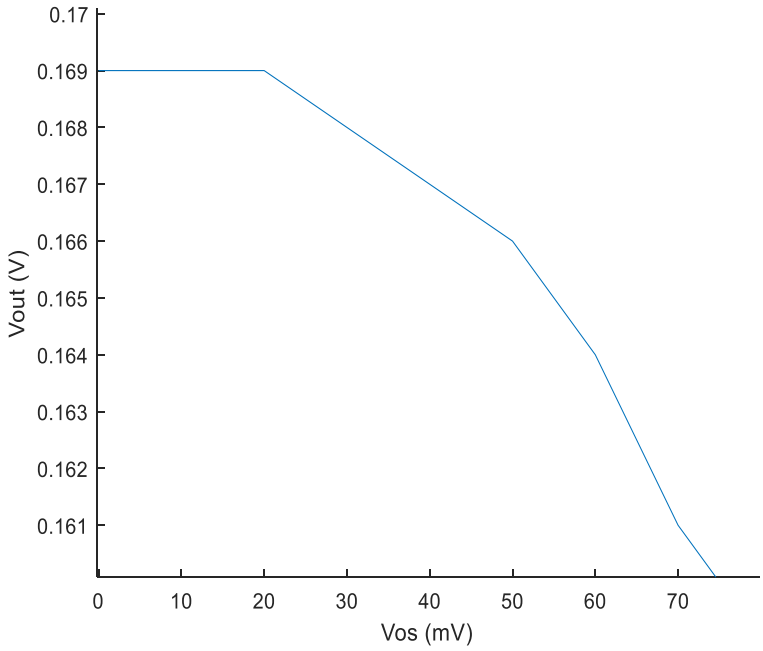


Figure 76: Simulated RMS output-noise of the RF power detector

Input Offset Input DC offset simulation was realized by placing a DC voltage source was at the first stage of the cascaded limiting amplifier's input to validate the operation of the DC offset cancellation circuit.



(a)



(b)

Figure 77: Effects of DC offset voltage on the transfer function of the RF power detector

Figure 77 (a) shows the transfer function of the RF power detector when the offset voltage is varied from 0 mV to 75 mV with a step size of 25 mV. As shown in Figure 77 (a), the RF power detector still operates appropriately even though an offset voltage of up to 75 mV is added to the first stage cascaded limiting amplifier input. Figure 74 (b) shows the effects of the offset voltage on the output of the RF power detector when an input power of -25 dBm at 2 GHz. As shown in Figure 74 (b), the output voltage of the RF power detector changes slightly when the DC offset voltage is varied from 0 to 75 mV, which validates the operation of the DC offset cancellation circuit.

Monte Carlo Analysis A series of simulations have been run to demonstrate mismatch effects on the power detector. Figure 78 shows the power detector's output voltage distribution produced by a Monte Carlo simulation for a -20 dBm 2 GHz input signal across 500 runs. The mean and standard deviation of the output voltage for a -20 dBm 2 GHz input signal is 0.277 V and 0.0039 V, respectively.

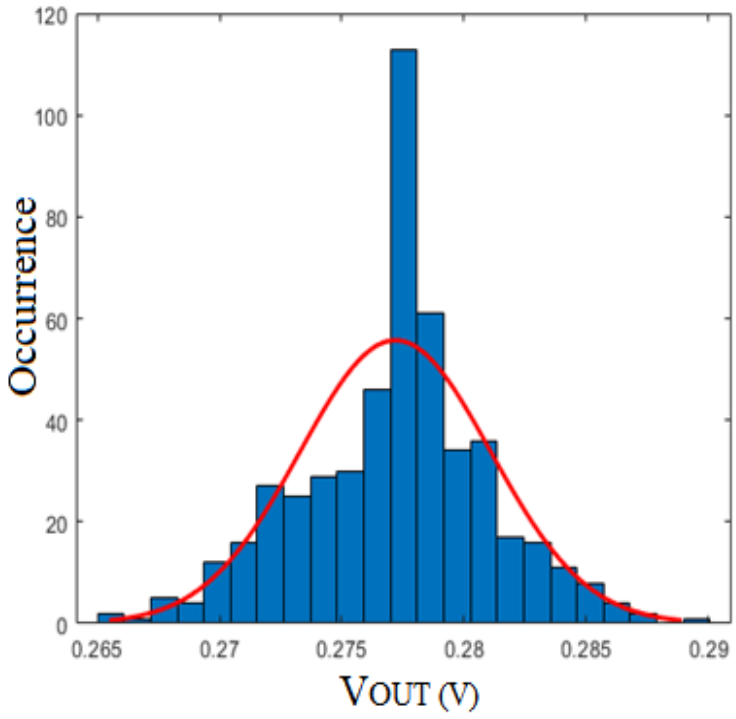


Figure 78: RF power detector Monte Carlo histogram simulation across 500 runs analysing mismatch effects on the output voltage for a -20 dBm 2 GHz input signal

Table 11 shows the detailed specifications of the proposed linear-in-decibel RF power detector.

Table 11: Specification summary for the power detector

Parameter	*Min*	*Typ*	*Max*	*Unit*
Operating Frequency f	2		4	[GHz]
Dynamic Range DR		40 (2 GHz) 30 (4 GHz)		[dB]
Input Power P_{IN}	-50		0	[dBm]
Relative Power Accuracy For 1 dB Power Step		±2		[dB]
Operating Temperature T	0	27	85	[°C]
Supply Voltage V_{DD}		1.8	2.2	[V]
Supply Current I_{DD}			0.35	[mA]

5.4. Performance Comparison

Several commercial power detectors are currently fabricated by top semiconductor companies, such as Analog Devices, Linear Technology, and Texas Instruments, available on the market. The RF power detectors from these companies are mostly fabricated using bipolar technologies, which offer better performance at the expense of higher power consumption. Thus, this research proposed RF power detector is primarily compared to a recently published RF power detector fabricated in CMOS technologies for more meaningful analysis.

Table 12 compares the proposed RF power detector's performances in terms of the operating frequency, dynamic range, and power consumption with other reported CMOS power detectors. In comparison to reference [4], which also uses an RMS detector to perform power detection but utilizes an exponential generator to provide linear-in-decibel output, the proposed power detector offers better sensitivity and higher dynamic range at the expense of higher power consumption. The reason is that exponential generator transistors limit the highest detectable signal.

Furthermore, compared to reference [25], which employed millimeter-wave amplifiers instead of limiting amplifiers for the gain cells to solve the limited amplifier's limited bandwidth, the proposed power detector offers lower power dissipation, comparatively similar sensitivity, and dynamic range. However, since the limiting amplifier's input is DC, wide bandwidth is unnecessary for this research. The proposed RF power detector offers comparatively low power consumption, a wide dynamic range, and adequate input power detectable range suitable for wireless communication and sensing devices in the agricultural sector.

Table 12: Comparison of existing power detector architecture

Parameters	**This work**	**(Chou et al. 2017)**	**(Zhou & Chia 2008)**	**(Kiela, Jurgo & Navickas 2013)**
CMOS Technology (nm)	180	90	130	65
Dynamic Range (dB)	40 (2 GHz), 30 (4 GHz)	50 (52 GHz), 37 (60 GHz)	20	65
Min. detectable signal (dBm)	-50	-50 (52 GHz), -35 (60 GHz)	-35	-80
Operating frequency (GHz)	2-4	52-60	0.125-8.5	-
Supply Voltage (V)	1.8	-	1.2	1.2
P_{DP}(mW)	0.61	20	0.18	24

5.5. Summary

This chapter delved into the simulation, testing, and evaluation of the proposed RF power detector using standard 180 nm CMOS process parameters. The BSIM3V1 MOSFET transistor model for integrated circuit design was employed to design the RF power detector. The proposed RF power detector design was developed using the Keysight Advanced Design System (ADS) version 2019 simulation software. Several simulations were run on each block of the RF power detector core to validate its operation. A transient simulation was carried to analyse transient voltage and the response time at each node of the RF power detector. Several DC simulations were also carried out to investigate the DC operation characteristics of the MOSFET and whether they are biased in the adequate inversion region. The effects of input offset voltage were also simulated through several DC simulations. It was found that the RF power detector still functions accurately for an input offset voltage of up to 75 mV. The frequency response of each block of the RF power detector was verified through a series of AC simulations. From the frequency response, the gain, the 3 dB cut-off frequency, roll-off frequency, and bandwidth were analysed and compared to hand calculation to validate the simulation result. The roll-off frequency of each block was used to locate the system's poles and zeroes and evaluate the system transfer function. Harmonic balance simulations were carried out using a power source to analyse the transfer characteristics of the proposed RF power detector from 2 GHz to 4 GHz. The simulated results showed that the RF power detector could input power from -60 dBm to 0 dBm with a dynamic range of 40 dB at 2 GHz and 30 dB at 4 GHz. Various simulations were also carried out to verify the operation of the RF power detector under temperature and supply variations. The simulation results demonstrate that the power detector operates appropriately for a temperature range of 0 °C to 85 °C, which suits application requirements. A series of Monte Carlo simulations were also run on the output voltage of the RF power detector to analyse the effect of mismatch and process variation. The performance metrics of the RF power detector were then compared to recently published research.

Chapter 6

Conclusion and Discussion

6.1. Introduction

This research focuses on designing and investigating a linear-in-decibel RF power detector operating in the S-band frequency range. This research was centered mainly on RF power detector design using CMOS technologies which offer lower cost and ultra-low power dissipation. The new circuit diagram of the RF power detector is shown in the Figure 79. The RF power detector was designed and simulated using standard 180 nm CMOS process parameters. The simulation results of the performance metrics such as operating frequency, dynamic range, sensitivity, and power consumption were analysed and compared to the recent CMOS RF power detectors.

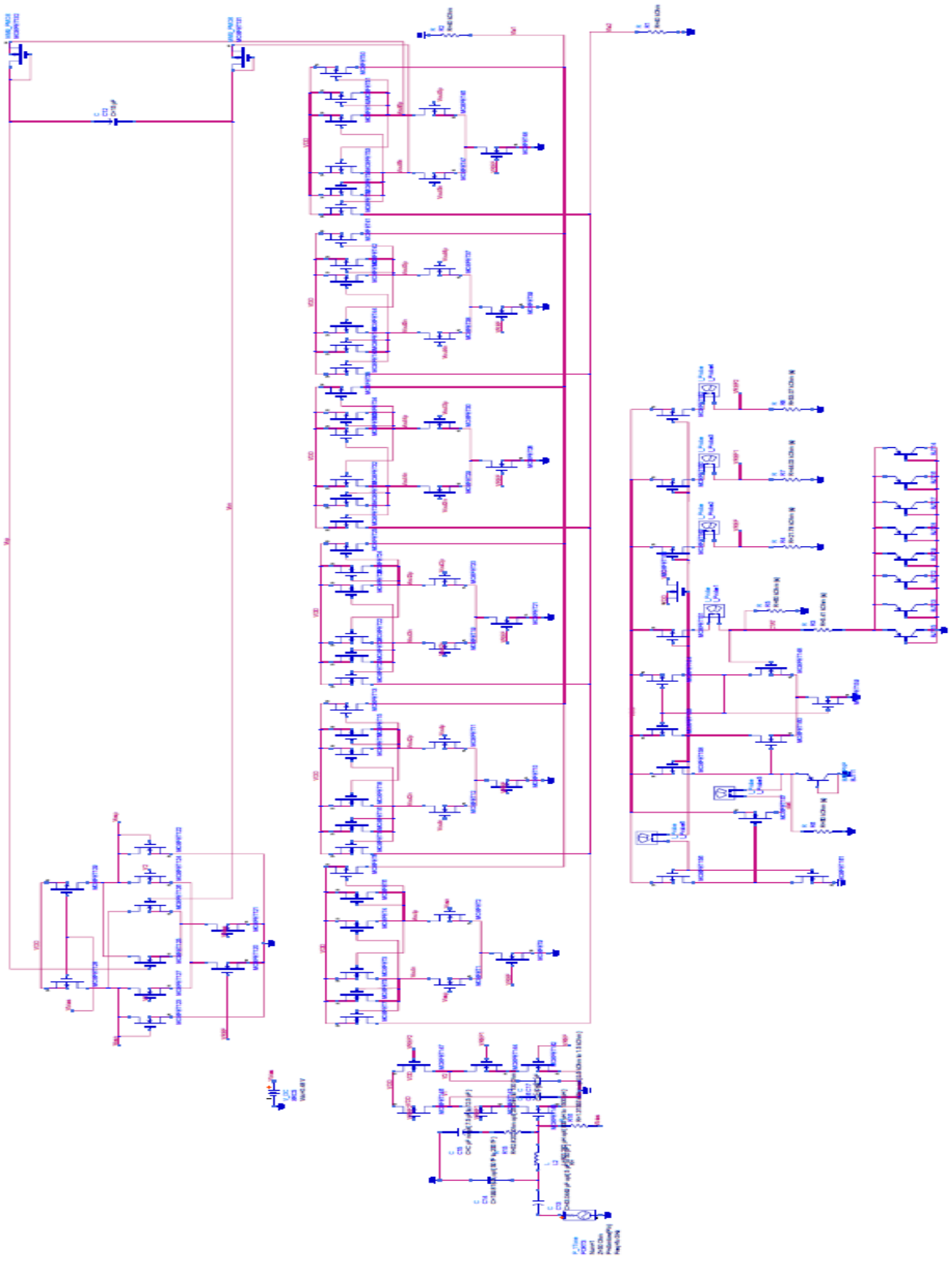


Figure 79 : The new circuit diagram of the FR power detector

6.2. Contributions

The objectives set in section 1.3 for this research was successfully completed and depicted from section 2 to 5. The contribution of each research objective is detailed below.

6.2.1. Research Objective 1: To implement and design a low-power linear-in-decibel RF power detector capable of reading up to 4 GHz.

The first objective for this study relates to the implementation and design of the RF power detector using CMOS technology for application in the S-band frequency range (2 GHz - 4 GHz). Since, currently, there are various types of RF power detectors, a review of the different RF power detectors design was carried out to establish their advantage and limitations. Based on the review of the RF power detectors and the targeted applications, logarithmic amplifiers preceded by an RMS detector were employed in this research to generate a high dynamic range linear-in-decibel output. This design's advantages are that since the input of the logarithmic amplifier is a DC voltage, rectifiers can be omitted, thereby reducing the total power consumption considerably. The RF power detector was successfully designed and simulated using the 180 nm CMOS technology parameters through Keysight Advanced Simulation Software (ADS). The simulation results showed that the proposed RF power detector generates linear-in-decibel output and accurately reads the RF input signal for frequencies up to 4 GHz. Comparing the proposed RF power detector with other detectors from literature indicated comparatively low power consumption, a wide dynamic range, and adequate input power detectable range suitable for wireless communication and sensing devices in the agricultural sector. As a result of the lack of low-power wide dynamic range linear-in-decibel RF power detectors and the challenges in implementing them, the proposed design provides critical research improvements regarding the design and implementation of linear-in-decibel RF power detectors.

6.2.2. Research Objective 2: To analyse the characteristics and critical parameters of linear-in-decibel RF power detectors via CMOS technology.

The RF power detector input-output characteristics and other critical parameters were verified and analysed through various simulations to determine if all design specifications are met under all operating conditions. The simulation results showed that the preceding RMS detector improves the sensitivity of the RF power detector by approximately 20 dB. Simulation results have shown that the RF power detector can operate appropriately under a range of temperature and supply variations. Series Monte Carlo simulations also demonstrated that the proposed

power detector is robust against parameter mismatch. The simulations also showed that regarding offset voltage which can affect the operation of the logarithmic amplifiers, the RF can still operate accurately for an input offset voltage up to 75 mV. The proposed RF power detector shows a wide dynamic range of 40 dB (2 GHz) and 30 dB (4 GHz), a minimum detectable input of -50 dBm, and a total power dissipation of 0.61 mW. The proposed design offers a considerably lower power dissipation when compared to recent linear-in-decibel RF power detectors involving logarithmic amplifiers. Despite a few limitations, the proposed RF power detector critical parameters meet the design specification set for the targeted applications.

6.2.3. Research Objective 3: Analyze the noise characteristics of the linear-in-decibel RF power detector.

Noise affects the accuracy of the RF power detector and can cause severe distortions to the output voltage. The targeted application of the proposed power detector requires a minimum noise level to maintain the sensitivity and accuracy at a low input signal level. In addition, for RF power detectors employed using cascaded limiting amplifiers, noise at the input can saturate the amplifier leading to inaccuracy at the output. In this research, several design techniques such as optimum sizing and biasing were adopted to minimize noise for each RF power detector's functional block. The simulated noise level of the first stage limiting amplifier is 250 nV over a 5 MHz bandwidth, while that of the RF power detector is 5 µV over a bandwidth of 70 MHz. In addition, the Noise Figure of the RF power detector was less than 10 dB from 2 GHz to 4 GHz. The noise simulation results established that the RF power detector has a low noise level adequate for reliable performance in wireless communications.

6.3. Limitations

This research comprised designing and implementing a low-power linear-in-decibel RF power detector and its performance evaluation through CMOS technology processes. Even though the RF power detector was designed and implemented successfully, there were still limitations to the design. During the design and implementation stage, several limitations happened regarding the capability of the simulation software Keysight ADS. Such limitations include a shortage of interactive tools for in-depth RFIC simulations and important DC operating parameters of MOSFET (example: μ_n and C_{ox} .) unavailability in the simulation window. Furthermore, the complexity of simulating and plotting the MOSFET process parameters' electrical and physical behaviour has made biasing of MOSFETs accurately in the different inversion regions difficult.

Another major limitation for the design and implementation of the RF power detector is that a Predictive Technology Model (PTM) was employed as process parameters for the 180 nm CMOS technology node. This PTM offers predictive, customizable, and accurate model files for interconnect technologies and future transistors. However, these PTM model files can be used for simulation and not for fabrication. This is a significant limitation because a successful chip design of the RF power detector would have further validated the simulation results and the robustness of the design. This inability to access model files from a foundry to fabricate the RF power detector chip using the 180 nm CMOS process is due to financial limitations and the prevailing pandemic.

6.4. Recommendations

6.4.1. Increasing the bandwidth of the RMS detector

The input-output characteristics of the linear-in-decibel RF power detector, as discussed in section 5.3, change as the frequency increases from 2 GHz to 4 GHz. More precisely, the output voltage of the RF power detector decreases as the frequency increases for the same input RF signal power. As discussed, prior this is due to the declining gain of the RMS detector as frequency increases. As such, to alleviate these issues, an RMS detector with a wider bandwidth is recommended.

6.4.2. Limiting amplifier power consumption optimization

As mentioned in the prior section, there are several limitations regarding the software Keysight ADS capabilities to perform complex RFIC and MOSFET characterization. Therefore, another recommendation would be to use another software such as Cadence with more capabilities which would help to optimize noise and power consumption design further. This is because, with the gm/id techniques, the transistors' dimensions and the region of operation can be determined precisely, thus enhancing the accuracy of the RF power detector.

6.4.3. Temperature and voltage variation stabilization

As mentioned in section 5, the temperature and voltage variation for the RF power detector is within the commercial standard (0 °C to +85 °C), but we recommend improving that to industry standards (-40 °C to +85 °C). This could be done by enhancing the temperature and voltage dependence of the voltage reference circuits. More accurate and better temperature-compensated design techniques instead of the bandgap voltage reference could be employed.

6.4.4. Implementation using a foundry CMOS process parameter.

Instead of using PTM files to model the transistors, we recommend using CMOS process parameters from a foundry. Using foundry process parameters facilitates the design and implementation of the RF power detector since foundries usually provide the user with Process Development Kits (PDKs) required helpful for the complete design, including schematic capture, layout planning, and IC fabrication.

6.5. Summary

Chapter 6 details how the various research aims and objectives of this study were successfully completed. The first objective was achieved by designing and implementing a low-power linear-in-decibel RF power detector for application in the S-band frequency range using CMOS technology. Then, the RF power detector's critical performance metrics were investigated to establish whether they met design specifications per application required, hence fulfilling the second objective. The third objective was also successfully completed through an in-depth analysis of the noise characteristics of the RF power detector. This chapter also presented some of the limitations of this study, which revolve around the software capabilities and the RF power chip fabrication. Several recommendations to improve the accuracy and performance of the RF power detector are also mentioned.

References

Aa, F 2006, 'An RF (R) MS Power Detector in Standard CMOS,'

Akin, T 2005, 'CMOS-based Thermal Sensors', *CMOS—MEMS*, pp. 479-512.

Al-Absi, MA & As-Sabban, IA 2014, 'A CMOS current-mode squaring circuit free of error resulting from carrier mobility reduction', *Analog Integrated Circuits and Signal Processing*, vol. 81, no. 1, 2014/10/01, pp. 23-28.

Ayed, A, Ghariani, H & Samet, M 2005, 'Design and optimization of CMOS OTA with gm/Id methodology using EKV model for RF frequency synthesizer application,' *2005 12th IEEE International Conference on Electronics, Circuits and Systems*, 1-5.

Bae, W 2019, 'CMOS Inverter as Analog Circuit: An Overview', *Journal of Low Power Electronics and Applications*, vol. 9, no. 3, p. 26.

Bahrami, E & Shamsi, H 2015, 'Ultra-low-power front-end CMOS true logarithmic amplifier for biopotential signal acquisition applications,' *2015 23rd Iranian Conference on Electrical Engineering*, 1230-1234.

Baker, RJ & Boyce, C 2005, 'Circuit design, layout, and simulation', in *IEEE Press Series on Microelectronic Systems*.

Bakker, A & Huijsing, JH 1996, 'Micropower CMOS temperature sensor with digital output', *IEEE Journal of Solid-State Circuits*, vol. 31, no. 7, pp. 933-937.

Banagozar, S & Yargholi, M 2019, 'Ultra-low power two-stage class-AB recycling double folded cascode OTA', *AEU-International Journal of Electronics and Communications*, vol. 110, p. 152848.

Barber, WL & Brown, ER 1980, 'A true logarithmic amplifier for radar IF applications', *IEEE Journal of Solid-State Circuits*, vol. 15, no. 3, pp. 291-295.

Bi, S, Lyu, J, Ding, Z & Zhang, R 2019, 'Engineering radio maps for wireless resource management', *IEEE Wireless Communications*, vol. 26, no. 2, pp. 133-141.

Bisdounis, L, Nikolaidis, S & Koufopavlou, O 1998, 'Analytical transient response and propagation delay evaluation of the CMOS inverter for short-channel devices', *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 302-306.

Bitzer, J, Schmidt, D & Simmer, U 2006, 'Parameter estimation of dynamic range compressors: models, procedures and test signals,' *Audio Engineering Society Convention 120*, Audio Engineering Society,

Bleeker, VR 2012, 'A Continuous Calibration Method For the Transfer Stabilization of Successive Detection Logarithmic Amplifiers,'

Brush, AS 2007, 'Measurement of microwave power - A review of techniques used for measurement of high-frequency RF power', *IEEE Instrumentation & Measurement Magazine*, vol. 10, no. 2, pp. 20-25.

Byun, S 2014, 'Analysis and Design of CMOS Received Signal Strength Indicator', *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 10, pp. 2970-2977.

Calvo, C & Pilotte, M 2006, 'RF power detection: Measuring WiMAX signals', vol. 49, 09/01, pp. 104-116.

Caylor, SD 2007, *A Standard CMOS Compatible Bandgap Voltage Reference with Post-Process Digitally Tunable Temperature Coefficient*, thesis, University of Tennessee, pp. 53.

Chauhan, HK, Tiwari, NK & Singh, SP 2017, 'Improved complementary split-ring resonator for nondestructive testing of materials,' *2017 4th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON)*, 370-375.

Chen, J-D 2013, 'A Low-Power Ultrawideband Low-Noise Amplifier in 0.18 μm CMOS Technology', *Active and Passive Electronic Components*, vol. 2013, 2013/12/24, p. 953498.

Choi, J, Lee, J, Xi, Y, Myoung, S, Baek, S, Kwon, DH, Bui, Q, Lee, J, Oh, D & Cho, TB 2016, 'Wide Dynamic-Range CMOS RMS Power Detector', *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 3, pp. 868-880.
Chokchalermwat, P & Supmonchai, B 2018, 'Design of a CMOS Low-Power Limiting Amplifier with RSSI Integrated Circuit for Low-Frequency Wake-Up Receivers,' *2018 International Electrical Engineering Congress (iEECON)*, 1-4.
Chou, C, Lai, W, Huang, T & Chuang, H 2017, 'A low minimum detectable power, high dynamic range, V-Band CMOS millimeter-wave logarithmic power detector,' *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 642-645.
Chun-Pang, W & Hen-Wai, T 2005, 'A 110-MHz 84-dB CMOS programmable gain amplifier with integrated RSSI function', *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1249-1258.
Cisco 2018, *Cisco Predicts More IP Traffic in the Next Five Years Than in the History of the Internet*, viewed <https://newsroom.cisco.com/press-release-content?type=webcontent&articleId=1955935>.
Cisco 2020, *Cisco Annual Internet Report (2018–2023) White Paper*, viewed <https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html>.
Comer, DJ & Comer, DT 2004, 'Using the weak inversion region to optimize input stage design of CMOS op amps', *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 1, pp. 8-14.
Counts., CKaL 1986, *RMS to DC conversion application guide 2nd Edition.*, viewed <http://www.analog.com/static/imported-files/design_handbooks/17505283758302176206322RMStoDC_Cover-Section-I.pdf >.
Cowles, JC 2004, 'The evolution of integrated RF power measurement and control,' *Proceedings of the 12th IEEE Mediterranean Electrotechnical Conference (IEEE Cat. No.04CH37521)*, 131-134 Vol.1.
Derafshi, ZH & Frounchi, J 2014, 'Low-noise low-power front-end logarithmic amplifier for neural recording system', *International journal of circuit theory and applications*, vol. 42, no. 5, pp. 437-451.
Detectors, viewed <http://www.tscm.com/detector.pdf>.
Devices, A 2004, *AD8361 LF to 2.5 GHz TruPwrTM Detector*, viewed <www.analog.com>.
Devices, A 2008, 'ADL5513 datasheet',
devices, A August 2017, *ADL5513, 1 MHz to 4 GHz, 80 dB Logarithmic Detector/Controller*, viewed <www.analog.com>.
Devices., A 2011.
Enz, C, Krummenacher, F & Vittoz, EA 1995, 'An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications', 01/01
Erikson, H & Waugh, RW June 2000, 'A temperature compensated linear diode detector ', pp. 40 - 44.
Fei, LF 2007, *Integrated power detector solutions and design strategies*, EE Times, viewed 14/02, <https://www.eetimes.com/integrated-power-detector-solutions-and-design-strategies/#>.
Ferrari, G, Prati, E, Fumagalli, L, Sampietro, M & Fanciulli, M 2005, 'Microwave power detector based on a single MOSFET in standard technology,' *2005 European Microwave Conference*, 4 pp.-1210.
Genest, P, Grandry, H, Chaoui, H & Semiconductor, O 2004, 'Criteria for Selecting RF Power Detectors', *High Frequency Electronics*, vol. 3, pp. 52-55.
Gilbert, B 'Noise Figure and Logarithmic Amplifiers [The Wit and Wisdom of Dr. Leif—6]',
Gray, PR 2009, *Analysis and design of analog integrated circuits,* 5th edn*.,* Wiley, New York.
Guglielmi, E, Toso, F, Zanetto, F, Sciortino, G, Mesri, A, Sampietro, M & Ferrari, G 2020, 'High-Value Tunable Pseudo-Resistors Design', *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2094-2105.
Hao, X, Zheng, Y, Tian, F, Zhou, Q, Li, H, Liu, Z, Liu, J & Liao, H 2019, 'A Reverse-RSSI Logarithmic Power Detector With+ 35-dBm Maximum Detectable Power in 180-nm CMOS', *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 9, pp. 610-613.

Harrison, RR & Charles, C 2003, 'A low-power low-noise CMOS amplifier for neural recording applications', *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958-965.
Helhel, S, Göksu, H & Ozen, S 2008, 'INVESTIGATION OF GSM SIGNAL VARIATION: DRY AND WET EARTH EFFECTS', *Progress In Electromagnetics Research B*, vol. 1, 10/09, pp. 147-157.
Holdenried, CD, Haslett, JW, McRory, JG, Beards, RD & Bergsma, AJ 2002, 'A DC-4-GHz true logarithmic amplifier: theory and implementation', *IEEE Journal of Solid-State Circuits*, vol. 37, no. 10, pp. 1290-1299.
Huang, P 1998, 'Analog front-end architecture and circuit design techniques for high speed communication VLSIs', *PHD's thesis, National Central University*,
Huang, Y, Yang, T, Hsu, S, Chen, X & Chiou, J 2015, 'A novel pseudo resistor structure for biomedical front-end amplifiers,' *2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2713-2716.
Ka Nang, L & Mok, PKT 2002, 'A sub-1-V 15-ppm//spl deg/C CMOS bandgap voltage reference without requiring low threshold voltage device', *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 526-530.
Kafe, F & Psychalinos, C 2014, '0.5 V RMS-to-DC converter topologies suitable for implantable biomedical devices', *Journal of Low Power Electronics*, vol. 10, no. 3, pp. 373-382.
Khan, SR 2018, 'Sub-1 V, 5.5 ppm/°C, High PSRR all CMOS Bandgap Voltage Reference', *IETE Journal of Research*, vol. 66, 07/19, pp. 1-6.
Kiela, K, Jurgo, M & Navickas, R 2013, 'Design of a Linear-in-dB Power Detector in 65nm CMOS Technology', *Electronics and Electrical Engineering*, vol. 19, 12/16, pp. 91-94.
Kitchin, C & Counts, L 1983, *RMS to DC Conversion Application Guide,* Analog Devices.
Kuphaldt, TR 2011, *Lessons in Electric Circuits Vol. 6 Experiments,* Koros Press Limited, United Kingdom.
Lee, S-H, Song, Y-H & Nam, S-W 2009, 'A fast RSSI using novel logarithmic gain amplifiers for wireless communication', *JSTS: Journal of Semiconductor Technology and Science*, vol. 9, no. 1, pp. 22-28.
Lee, S, Song, Y & Nam, S 2008, 'Fast RSSI circuit using novel power detector for wireless communication,' *2008 International SoC Design Conference*, I-9-I-12.
Li, C, Gong, F & Wang, P 2010, 'A Low-Power Ultrawideband CMOS Power Detector With an Embedded Amplifier', *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 12, pp. 3270-3278.
Li, C, Yi, X, Boon, CC & Yang, K 2019, 'A 34-dB Dynamic Range 0.7-mW Compact Switched-Capacitor Power Detector in 65-nm CMOS', *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9365-9368.
Liao, C, Li, J & Li, S 2017, 'Design of LCC impedance matching circuit for wireless power transfer system under rectifier load', *cpss transactions on power electronics and applications*, vol. 2, no. 3, pp. 237-245.
Lund, H 2006, *IV and CV characterization of 90nm CMOS transistors*, thesis, Institutt for elektronikk og telekommunikasjon.
Microwaves101 2021, *Voltage standing wave ratio (VSWR)*, viewed <https://www.microwaves101.com/encyclopedias/voltage-standing-wave-ratio-vswr>.
Milanovic, V, Gaitan, M, Marshall, JC & Zaghloul, ME 1996, 'CMOS foundry implementation of Schottky diodes for RF detection', *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2210-2214.
Mohammed, M, Abugharbieh, K, Suliman, M & Kawar, S 2016, 'Design Methodology for MOSFET-Based Voltage Reference Circuits Implemented in 28nm CMOS Technology', *AEU - International Journal of Electronics and Communications*, vol. 70, 01/25
Moody, J, Bassirian, P, Roy, A, Liu, N, Barker, NS, Calhoun, BH & Bowers, SM 2019, 'Interference robust detector-first near-zero power wake-up receiver', *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2149-2162.
Muijs, E 2013, 'A CMOS Temperature Compensated Log-Amp Detector',
Muijs, E, Silva, P, Staveren, Av & Serdijn, W 2013, 'A 39 dB DR CMOS log-amp RF power detector with ±1.1 dB temperature drift from −40 to 85°C,' *2013 Proceedings of the ESSCIRC (ESSCIRC)*, 287-290.

Nash, E *Improving Temperature, Stability, and Linearity of High Dynamic Range RMS RF Power Detectors*, Anlog Devices, viewed 01/02, <https://www.analog.com/en/app-notes/an-653.html>.
Nash, E 1999, 'Logarithmic Amplifiers Explained', *Ask the Applications Engineer—28,*, vol. 33,
Nguyen, DP, Nguyen, NLK, Stameroff, AN, Camarchia, V, Pirola, M & Pham, A 2020, 'A Wideband Highly Linear Distributed Amplifier Using Intermodulation Cancellation Technique for Stacked-HBT Cell', *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 7, pp. 2984-2997.
Nielsen, TS, Lindfors, S, Tawfik, S & Larsen, T 2005, 'Modeling power amplifiers with antenna mismatch,' *2005 IEEE International Symposium on Circuits and Systems*, 5083-5086 Vol. 5.
Pedram, M 1996, 'Power minimization in IC design: principles and applications', *ACM Trans. Des. Autom. Electron. Syst.*, vol. 1, no. 1, pp. 3–56.
Pereira, CF, Benko, PL, Galeti, M, Lucchi, JC & Giacomini, RC 2017, 'Experimental study and modeling of pseudo-resistor's non-linearity,' *2017 32nd Symposium on Microelectronics Technology and Devices (SBMicro)*, 1-4.
Petrofsky, JG 2002, US Patent 6,359,576.
Petrović, PB 2015, 'A new high precision power detector of complex voltage signals', *Measurement Science Review*, vol. 15, no. 4, pp. 184-195.
Pinjare, SL, Nithya, G, Nagaraja, VS & Sthuthi, A 2018, 'A Gm/Id Based Methodology for Designing Common Source Amplifier,' *2018 2nd International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE)*, 304-307.
Piovani, DS & de Sousa, FR 2011, 'Analysis of a MOSFET operating as an RF power detector,' *2011 Argentine School of Micro-Nanoelectronics, Technology and Applications*, IEEE, 1-4.
Po-Chiun, H, Yi-Huei, C & Chorng-Kuang, W 2000, 'A 2-V 10.7-MHz CMOS limiting amplifier/RSSI', *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1474-1480.
Qayyum, S & Negra, R 2017a, '0.8 mW, 0.1–110 GHz RF power detector with 6 GHz video bandwidth for multigigabit software defined radios,' *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 1722-1725.
Qayyum, S & Negra, R 2017b, '0.16 mW, 7–70 GHz distributed power detector with 75 dB voltage sensitivity in 130 nm standard CMOS technology,' *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, 13-16.
Qayyum, S & Negra, R 2018, 'Analysis and Design of Distributed Power Detectors', *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 9, pp. 4191-4203.
Raab, FH, Asbeck, P, Cripps, S, Kenington, PB, Popovic, ZB, Pothecary, N, Sevic, JF & Sokal, NO 2002, 'Power amplifiers and transmitters for RF and microwave', *IEEE transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814-826.
Ramos, J, Ausín, J, Duque, F & Torelli, G 2011, *Design considerations on CMOS limiting amplifiers for wearable biomedical systems*.
Ramos, J, Ausín, JL, Duque-Carrillo, JF & Torelli, G 2010, 'Design of limiting/logarithmic amplifier for wideband bioimpedance measuring devices,' *2010 Biomedical Circuits and Systems Conference (BioCAS)*, 290-293.
Ratni, M, Huyart, B, Bergeault, E & Jallet, L 1998, 'RF power detector using a silicon MOSFET,' *1998 IEEE MTT-S International Microwave Symposium Digest (Cat. No.98CH36192)*, 1139-1142 vol.2.
Razavi, B 1999, 'CMOS technology characterization for analog and RF design', *IEEE Journal of Solid-State Circuits*, vol. 34, no. 3, pp. 268-276.
Reimann, R & Rein, H-M 1987, 'Bipolar high-gain limiting amplifier IC for optical-fiber receivers operating up to 4 Gbit/s', *IEEE journal of solid-state circuits*, vol. 22, no. 4, pp. 504-511.
Rizk, MRM, Abou-Bakr, E, Nasser, AAA, El-Badawy, EA & Mahros, AM 2016, 'On the investigation of voltage standing wave ratio to design a low noise wideband microwave amplifier,' *2016 Eighth International Conference on Ubiquitous and Future Networks (ICUFN)*, 568-572.

Sabry, MN, Omran, H & Dessouky, M 2018, 'Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology', *Microelectronics Journal*, vol. 75, 2018/05/01/, pp. 87-96.
Sakphrom, S & Thanachayanont, A 2012, 'A low-power CMOS RF power detector,' *2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012)*, 177-180.
Semiconductor, O 2006.
Sharma, VK & Soni, S 2010, 'Comparison among different CMOS inverter for low leakage at different technologies', *International Journal of Applied Engineering Research*, vol. 1, no. 2, p. 228.
Shieh, M-L, Lai, W-J, Li, J-S, Chiang, Y-L, Wu, H-H, Xsieh, C-C, Tu, C-H, Chen, S-W & Wu, J-W 2009, 'Linear radio frequency power detector,' *2009 Asia Pacific Microwave Conference*, IEEE, 2316-2319.
Shillady, RW 1986, 'HIGH DYNAMIC RANGE VIDEO DETECTOR', *IEEE MTT-S Int Microw. Symp. Dig*, pp. 301-304.
Skinner, A & Lambert, M 2009, 'A Log-Antilog Analog Control Circuit for Constant-Power Warm-Thermistor Sensors— Application to Plant Water Status Measurement', *IEEE Sensors Journal*, vol. 9, 10/01, pp. 1049-1057.
Stärke, P, Rieß, V, Fritsche, D, Carta, C & Ellinger, F 2017, 'A wideband square-law power detector with high dynamic range and combined logarithmic amplifier for 100 GHz F-Band in 130 nm SiGe BiCMOS,' *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, IEEE, 118-121.
Sundarasaradula, Y & Thanachayanont, A 2013, 'A 0.7-V, 2.86-µW low-noise logarithmic amplifier for neural recording system,' *2013 IEEE International Conference of IEEE Region 10 (TENCON 2013)*, 1-4.
Sundarasaradula, Y & Thanachayanont, A 2017, 'A Low-Noise, Low-Power, Wide Dynamic Range Logarithmic Amplifier for Biomedical Applications', *Journal of Circuits, Systems and Computers*, vol. 27, 11/01, p. 1850104.
Sunghyun, C & Pavon, JdP 2003, '802.11g CP: a solution for IEEE 802.11g and 802.11b inter-working,' *The 57th IEEE Semiannual Vehicular Technology Conference, 2003. VTC 2003-Spring.*, 690-694 vol.1.
Tao, Z, Eisenstadt, WR & Fox, RM 2004, 'A novel 5GHz RF power detector,' *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, I-897.
Thanachayanont, A 2015, 'Design of a low-power wide dynamic range CMOS RF power detector', *International Journal of Electronics Letters*, vol. 3, no. 4, pp. 213-224.
Valdes-Garcia, A, Venkatasubramanian, R, Silva-Martinez, J & Sanchez-Sinencio, E 2008, 'A Broadband CMOS Amplitude Detector for On-Chip RF Measurements', *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 7, pp. 1470-1477.
Vithanawasam, CK, Then, YL & Su, HT 2019, 'Design and Practical Implementation of Two-Port Network Analyzer for Microwave Measurement from 200 MHz to 2.7 GHz,' *2019 IEEE International Circuits and Systems Symposium (ICSyS)*, IEEE, 1-4.
Wang & Cao 2019, 'A Review of Impedance Matching Techniques in Power Line Communications', *Electronics*, vol. 8, 09/12, p. 1022.
Wang, J, Zheng, Y, Yang, F, Tian, F & Liao, H 2015, 'A wide band CMOS radio frequency RMS power detector with 42-dB dynamic range,' *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 1678-1681.
Wang, K, Lei, X, Ma, K, Yeo, KS, Cao, X & Wang, Z 2013, 'A CMOS low-power temperature-robust rssi using weak-inversion limiting amplifiers', *Journal of Circuits, Systems, and Computers*, vol. 22, no. 10, p. 1340034.
Wei, M, Qayyum, S & Negra, R 2016, 'High sensitivity tunable power detector,' *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 1-4.
Weste, NH & Harris, D 2015, *CMOS VLSI design: a circuits and systems perspective,* Pearson Education India.
White, J 2003, *High Frequency Techniques: An Introduction to RF and Microwave Engineering*.

World, RW 2012, *RF Detector Basics*, viewed 05/28, <https://www.rfwireless-world.com/Terminology/RF-detector.html>.
Wu, J, Hsu, K, Lai, W, To, C, Chen, S, Tang, C & Juang, Y 2011, 'A linear-in-dB radio-frequency power detector,' *2011 IEEE MTT-S International Microwave Symposium*, 1-4.
Xu, K, Yang, X, Wang, W & Yoshimasu, T 2014, '44-GHz, 0.5-V compact power detector IC in 65-nm CMOS,' *2014 IEEE International Wireless Symposium (IWS 2014)*, 1-3.
Yan, L & Kallfass, I 2018, 'Adopting the BSIM3 Model to Describe the DC-IV Characteristics of a Vertical Power MOSFET,' *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, IEEE, 1-6.
Yang, C & Mason, A 2008, 'Process/Temperature Variation Tolerant Precision Signal Strength Indicator', *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 3, pp. 722-729.
Yarman, BS 2010, *Design of ultra wideband power transfer networks,* John Wiley & Sons.
Yijun, Z & Wah, MCY 2006, 'A wide band CMOS RF power detector,' *2006 IEEE International Symposium on Circuits and Systems*, 4 pp.-4231.
Yingbo, D, Kefeng, H, Na, Y & Xi, T 2012, 'A high dynamic range linear RF power detector with a preceding LNA', *Journal of Semiconductors*, vol. 33, 01/01
Yong, Z, Lei, C, Xiao-jun, Z & Zong-sheng, L 2009, 'A parallel-amplification parallel-summation logarithmic amplifier for UHF RFID reader,' *2009 IEEE 8th International Conference on ASIC*, IEEE, 1121-1124.
Zareie, M, Hosseinnejad, M & Azhari, SJ 2019, 'Ultra-Low-Power, Wide Dynamic Range Front-End Logarithmic Amplifier for Biomedical Applications,' *2019 5th Conference on Knowledge Based Engineering and Innovation (KBEI)*, 548-552.
Zhang, J, Fusco, V & Zhang, Y 2012, 'A compact V-band active SiGe power detector,' *2012 7th European Microwave Integrated Circuit Conference*, 528-531.
Zhang, T, Eisenstadt, WR, Fox, RM & Yin, Q 2006, 'Bipolar Microwave RMS Power Detectors', *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2188-2192.
Zhou, Y & Chia, MY 2008, 'A Low-Power Ultra-Wideband CMOS True RMS Power Detector', *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1052-1058.
Zhu, M, Ma, J, Nela, L, Erine, C & Matioli, E 2019, 'High-voltage normally-off recessed tri-gate GaN power MOSFETs with low on-resistance', *IEEE Electron Device Letters*, vol. 40, no. 8, pp. 1289-1292.

Appendix A

The figures below illustrate example of the device size found in table 6 simulation optimization.

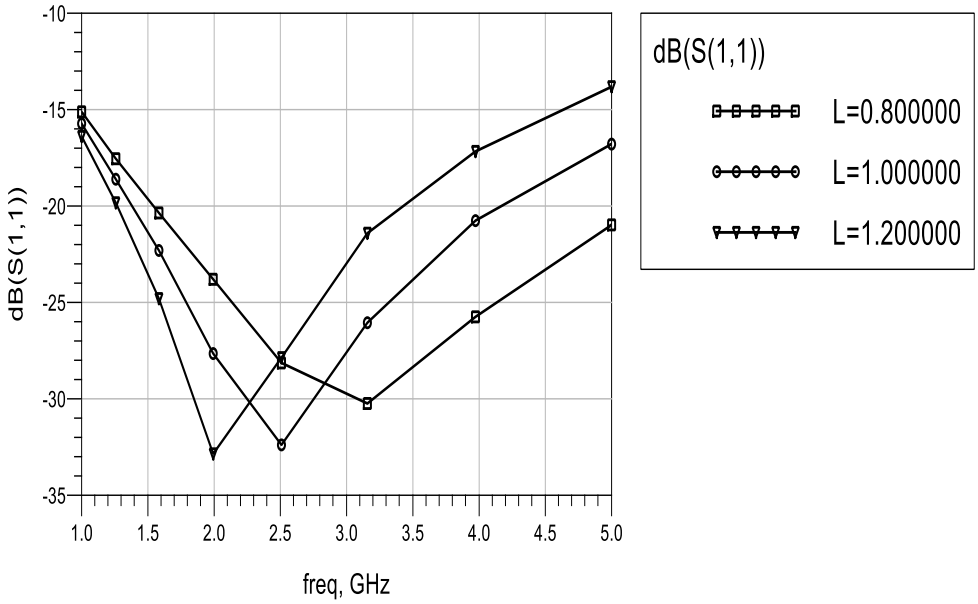


Figure A-1: Fixed $C1$, $C2$, $C3$ and $R1$ and simulated $L1$ variation input reflection coefficient.

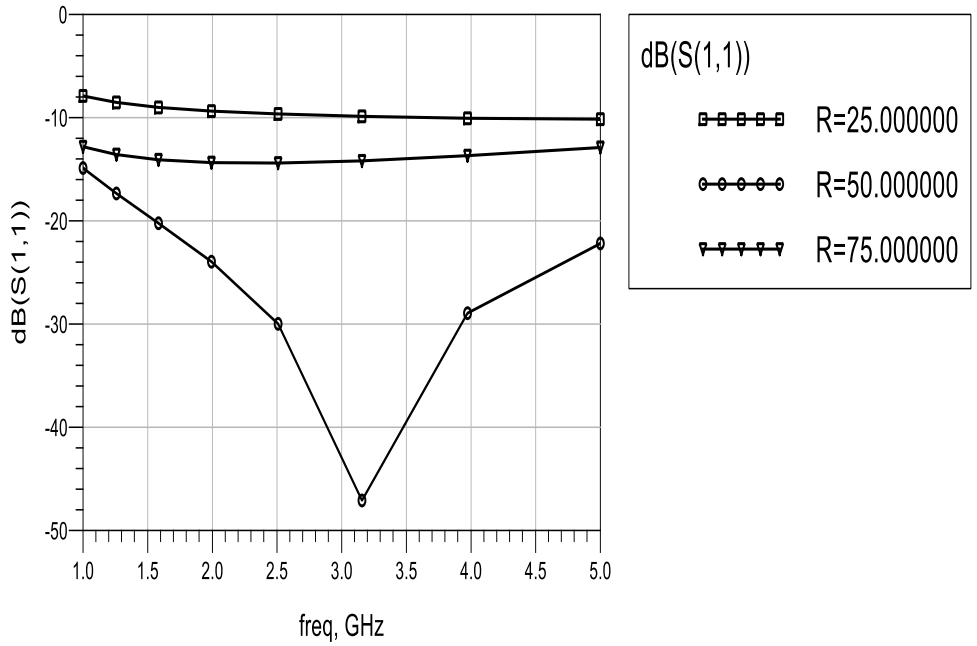


Figure A-2: Fixed $C1$, $C2$, $C3$, and $L1$ and simulated $R1$ variation input reflection coefficient

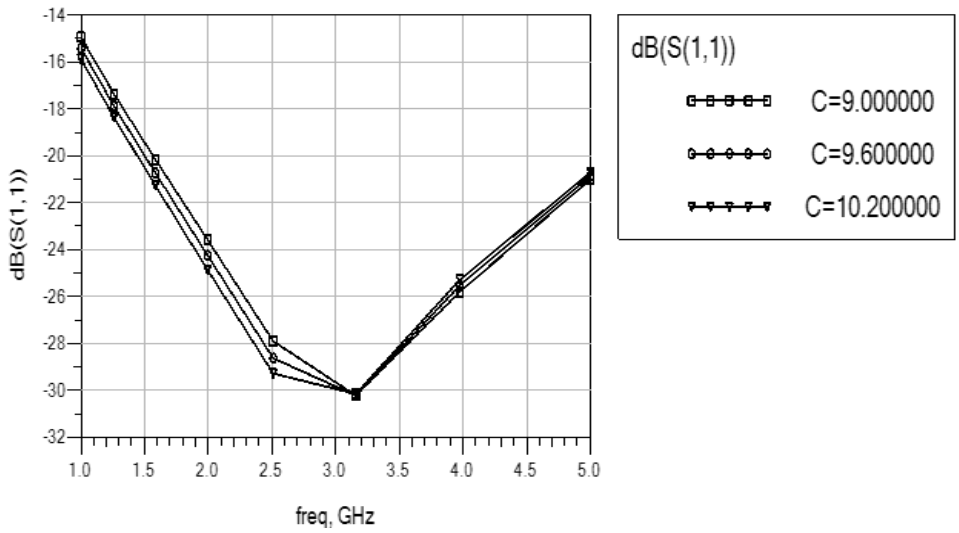


Figure A-3: Fixed $C1$, $C2$, $R1$, and $L1$ and simulated $C3$ variation input reflection coefficient.

Appendix B

B.1 Measurement Results (Breadboard Prototype)

As mentioned in sub-section 6.3, one of the major limitations of this research concerns the fabrication of the designed linear-in-decibel RF power detector using CMOS technology processes. Therefore, fabrication alternatives were proposed to implement the RF power detector and investigate its functionalities. According to the schematic capture, the first alternative is using power MOSFETs on breadboards to implement the RF power detector. Power MOSFETS are well-recognized semiconductors with different device geometry, voltage, and current levels. With the significant advancement in semiconductor manufacturability, power MOSFETs costs have been reduced considerably, improving their accessibility. Figure B-1 shows the simplified device structure of an N-channel power MOSFET.

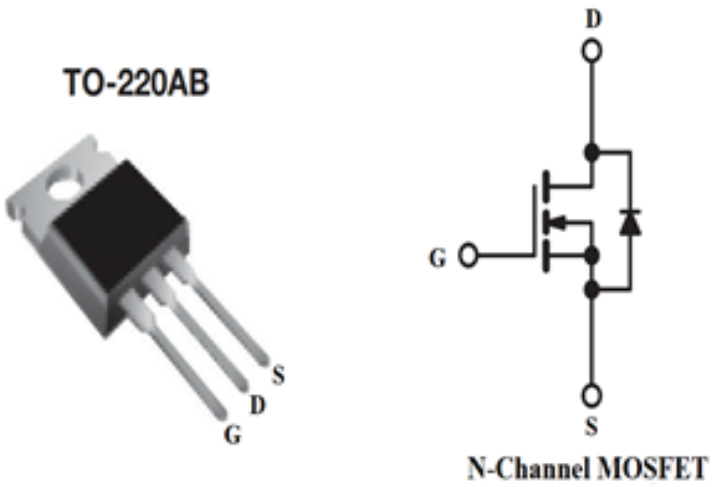


Figure B-1: Simplified device structure of N-channel Power MOSFET

The P-channel and N-channel power MOSFETs (Model: FQU11P06TU, and IRLZ14 SiHLZ14, respectively) were used to fabricate the RMS power detector because of their fast switching, robust design, and cost-effectiveness. In addition to that, the low on-resistance of the power MOSFET improves high-frequency operations (Zhu et al. 2019). The method in (Yan & Kallfass 2018) was used to extract the power MOSFETs parameters for simulation in Keysight ADS using the BSIM3 model to characterize the power MOSFETs. The simulation results from the vendor datasheets were employed to extract the parameters describing the power MOSFET operations. Figure B-2 shows the RMS power detector implementation on a breadboard using power MOSFETs, lumped elements, and jumper wires.

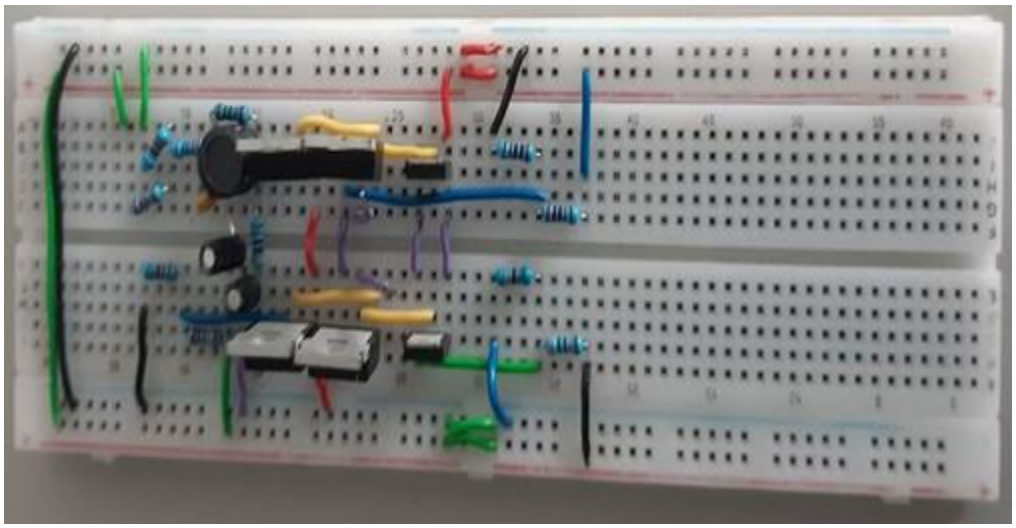


Figure B-2: Breadboard Implementation of the RMS Power Detector

Figure B-3 shows the measurement setup employed to investigate the RMS power detector characteristics. The RF signals were achieved using the SynthHD dual-channel signal generator, generating RF signals for the frequency ranges of 54 MHz to 13.6 GHz. LabView software in windows was utilized for generating the RF signals and running frequency sweeps. Due to the breadboard slots configurations, a handmade BNC – Pig Tail coaxial cable was used to connect the signal generator to the RMS power detector input. Then, the differential output voltage of the RMS power detector was measured using an oscilloscope while the input power was swept from -60 dBm to 0 dBm at 2 GHz, as shown in Figure B-3.

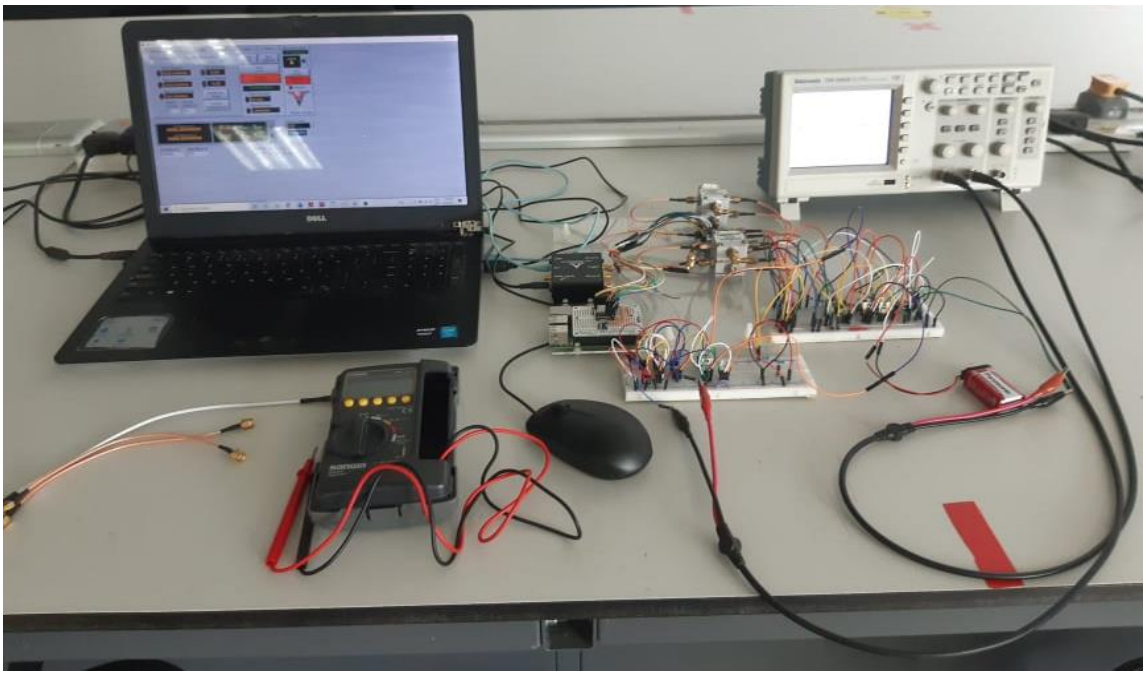


Figure B-3: The RMS power detector (breadboard) measurement setup

Figure B-4 shows the differential output voltage of the RMS power detector when the input power was swept from -60 dBm to 0 dBm at 2 GHz

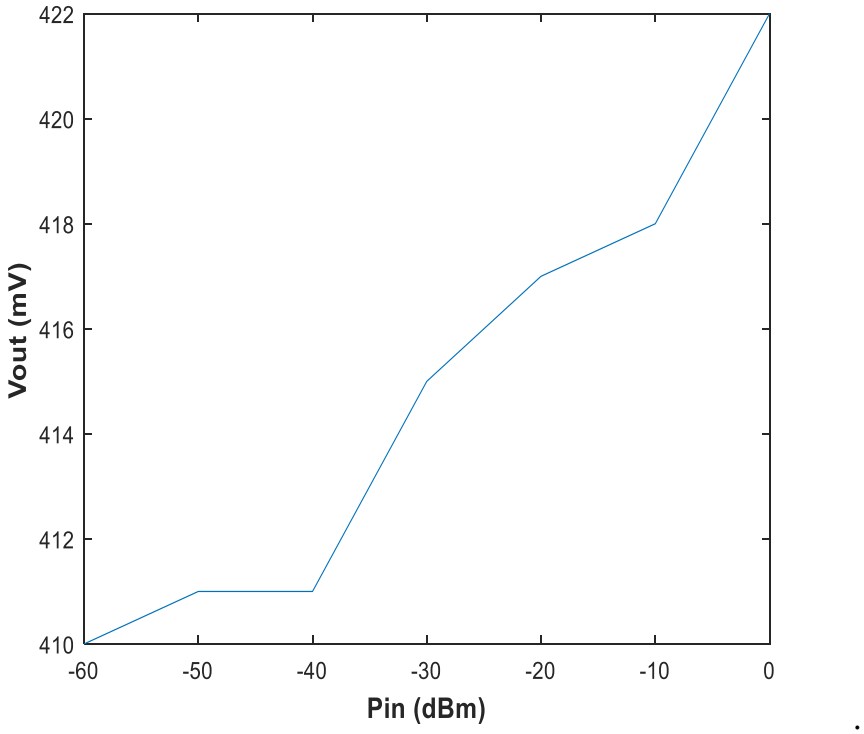


Figure B-4: The measured differential output of the RMS power detector unit at 2 GHz

As shown in Figure B-4, the differential output voltage of the RMS power detector does not represent the square-law characteristics of MOSFETs in the saturation region compared to the simulation results. The difference between the breadboard measurement and the simulation results might be because of the following:

1. *RF signal power loss through the direct connection between the signal generator and the breadboard.*

As mentioned prior, the connection between the signal generator and the breadboard is achieved with a BNC – Pig Tail coaxial cable. BNC – Pig Tail connection can result in significant RF power loss, explaining why the differential output voltage does not represent the square law principle as the input power is swept.

2. *The high-frequency operation*

For high-frequency circuit operation on breadboards, the signal coupling issues in the panel version must be overcome. For RF signals below 20 MHz, the RF coupling strength within one division is less than 40 dB. This is acceptable for most analogue and digital circuit experiments.

For high-frequency RF signals at 40 MHz and around 110 MHz, the coupling strength in the class is high. Especially for RF signals around 40 MHz that are one grid apart, the coupling loss between each other is only more than 10 dB, leading to greater interference for many analogue and digital signals. For the proposed RF power detector, which requires power detection in the S-band frequency range (considered as UHF), the breadboard measurement results at high frequencies are inaccurate mainly due to the following reasons:

- Long lead Lengths

Long lead lengths introduce undesirable capacitance, inductance, and resistance that negatively influence high-frequency circuit operation. The breadboard contacts introduce resistance.

- Power supply noise

A battery should not be an issue, yet AC to DC supply with poor filtering may introduce noise on the supply lines.

- The high Capacitance and inductance between the breadboard grids

During performance testing of the RF power detector, the capacitance and inductance between the grids of the breadboard were measured because they affect high-frequency circuit operation. The measurements showed a capacitance of 4 pF between each breadboard grid and 20 pF the power bus grid between the side-to-side grids. The capacitance between the breadboard grid considerably affects the high-frequency operation of the breadboard implementation. Considering the major limitation of breadboard at high-frequency operations, which resulted in inaccurate measurement results, a second alternative employing FR4 Veroboard instead of breadboard was proposed.

B.2 Measurement Results (FR4 PCB Prototype)

Due to the inaccuracy of the first alternative (Breadboard), we decided to implement the RMS power detector using the same power MOSFET on a piece of FR4 PCB. FR4 substrate was chosen because it can handle much higher frequency than breadboard and is also readily available. However, FR4 is considered a lossy PCB material for ultra-high frequency operation. Another significant advantage of FR4 PCB compared to a breadboard is a better connection from the signal generator via coaxial cable, reducing reflection and maximizing power transfer. Figure

B-5 shows the RMS power detector implementation on an FR4 PCB using power MOSFETs, lumped elements, and jumper wires.

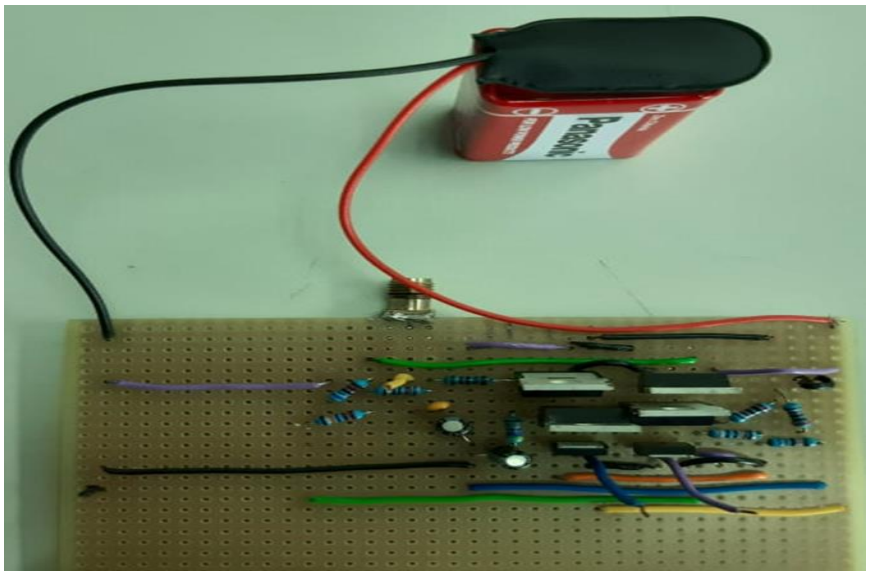


Figure B-5: FR4 PCB Implementation of the RMS Power Detector

Figure B-6 displays the same measurement setup as shown in Figure B-3, employed to investigate the characteristics of the RMS power detector implemented using the FR4 PCB.

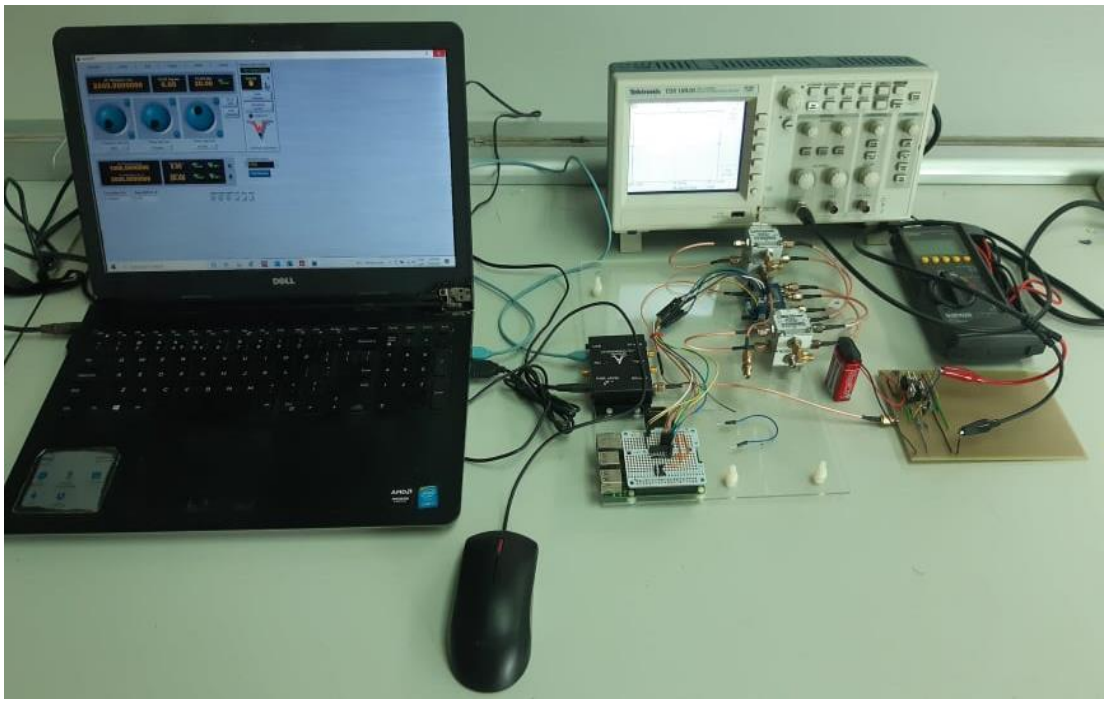


Figure B-6: The FR4 RMS power detector measurement setup

The main difference is that for the FR4 prototype, a regular BNC-BNC coaxial cable was employed to connect the signal generator to the RMS power detector. Figure B-7 shows the differential output voltage of the RMS power detector when the input power was swept from -60 dBm to 0 dBm at 2 GHz. As shown in Figure B-7, even though the measured differential output voltage of the RMS power detector implemented using the FR4 PCB is slightly better than the breadboard model, the results still do not represent the square-law characteristics of MOSFET in the saturation. However, we can conclude that the RF power detector implemented using power MOSFETs on an FR4 PCB for operation the S-band frequency range is a potential research area.

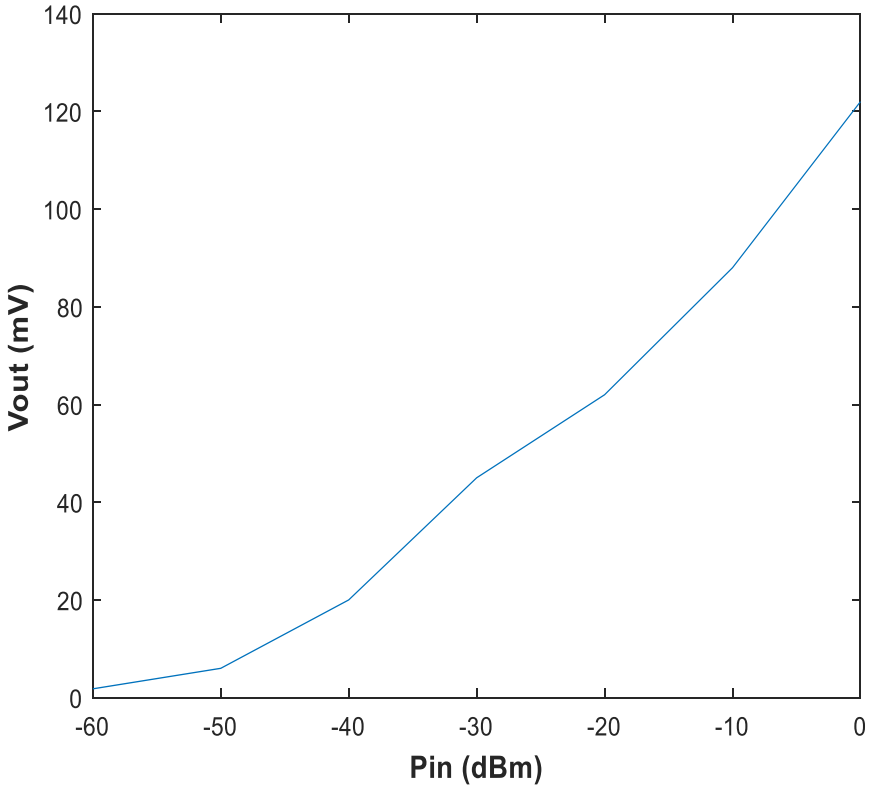


Figure B-7: The measured differential output of the RMS power detector unit at 2 GHz

Comparing the simulation results which employed CMOS process parameters and the measurement results which employed power MOSFETS, it is found that the respective transfer function differs. The main reasons for the difference between the simulations results and measured results might be explained as follows:

1. *The physical and electrical characteristics difference between the MOSFET model employed in simulations and the power MOSFET used for the measurement.*

   As mentioned prior, due to certain limitations, fabrication using 180 nm CMOS processes was not possible, as such power MOSFET was proposed as a proof of concept. The MOSFET dimensions employed for simulation are nanometres, whereas power MOSFETs used for the physical model are millimetres. This difference in dimensions affects the physical and electrical characteristics of the circuit design, thereby resulting in different results. Furthermore, since the electrical characteristic differs, other biasing and VDD were employed for the physical implementation. For instance, a VDD of 9 V was utilized for the FR4 PCB model instead of the 1.8 V used for simulation.

2. *The high dissipation factor of FR4 at high frequencies*

   FR-4 has a higher dissipation factor (Df) than laminates engineered for high-frequency applications. Even though FR-4 PCB shows better high-frequency operation than a breadboard, circuits fabricated on FR-4 still suffer higher losses than similar circuits formed on a high-frequency circuit.

The measured results of the differential output voltage of the RMS power detector implemented on FR4 PCB substrate show that power MOSFETs can detect RF power. However, due to the significant difference in physical and electrical characteristics between power MOSFETs and CMOS technologies parameters, the differential output voltage of each implementation differs.