Ultra Low Power, High resolution ADC for Biomedical Applications

L. Hiremath, V. Mallapur, A. Stojcevski, J. Singh, H.P. Le, A. Zayegh
Faculty of Science Engineering & Technology
Victoria University, P.O.BOX 14428, Melbourne City
MC 8001, Victoria, Australia

ABSTRACT

This paper presents a fully differential ultra low power successive approximation (SA) Analog-to-digital converter (ADC) for biomedical application. In order to reduce the system power consumption, the building block components of the SA ADC architecture has been opsimised. In addition, the ADC the input voltage swing is scaled down to in order to reduce the slope gain error and the nonlinearity errors. The SA ADC has been implemented in Cadence Analog Design Environment using 0.18-micron CMOS technology. The designed SA ADC operates at a sampling rate of 200S/s at 3V power supply and consumes only 12µW of power at this frequency. The ADC standby power consumption is less than 1µW. The designed 16-bit ADC occupies an area of 0.1 mm^2 and is the smallest in size among its 16-bit counter parts reported in the literature. The proposed 16-bit ADC achieves the differential-non-linearity (DNL) and integral-non-linearity errors (INL) of ± 0.5 LSB and ± 0.3 LSB respectively.

Keywords: Analog to digital (A/D) converter, Ultra low power, Successive approximation, CMOS analog integrated circuits, Low power comparator.

1. INTRODUCTION

The signal processing of biomedical application typically requires low voltage, low noise analog interfaces which places a high demand for very low power consumption and low cost analog-to-digital converter (ADC) [1]. Cardiac pacemaker, neural recordings, etc are becoming common practice in biomedical applications, for example implantable bioamplifiers must dissipate little power so that surrounding tissues are not damaged by heating. The existing ADC circuits have unacceptable noise levels or consume too much power to be fully implanted in a large quantity. On the other hand for high resolution ADC, a better precision component matching is required along with a high accuracy trimming techniques or self calibrating circuits for better linearity.

Successive Approximation (SA) ADC architectures are extremely suitable for low power and small area applications. The total power consumption has a linear relation with the sampling frequency. This means that for low frequency applications this architecture consumes extremely less power. The total silicon area used has a linear relation with the resolution; this makes this architecture area efficient. The SA ADC architecture is relatively less complex to implement compared to other architectures. The SA ADC architecture allows for high performance, low power ADCs to be packaged in small form factors for today's advanced biomedical applications.

At the simulation stages certain implementation issues may not arise as the design then works in ideal condition. Therefore a new circuit technique that improves the system accuracy is required. This paper presents a modified conventional SA ADC structure to achieve a high resolution and low power. The input voltage swing was scaled down to in order to reduce the slope gain error and the nonlinearity errors. A comparator is the most important component in the SA ADC since its input offset voltage, delay and input range directly influence the resolution and speed of the ADC. The dynamic latch comparator employed within ADC design has been modified to reduce power problem by removing the pre-amplifier stage. The comparator also occupies less area and achieves a better resolution with a smaller offset error. Such comparator enables a large reduction of the system power consumption and makes the ADC the perfect solution for biomedical applications.

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2. DESIGN AND IMPLEMENTATION OF THE SA ADC

The architecture has been implemented taking into account the typical constraints of a biomedical implantable application. The basic differential SA ADC structure has been modified in order to decrease the system power consumption and increase the system accuracy, taking advantage of certain unconventional ideas in order to meet the power specifications. The conventional SA ADC architecture is shown in Fig. 1. Initially, a time-muxed architecture has been implemented at the initial stage, however it requires a large area and consumes too much of power. To overcome this issue, an op-amp in subtractor mode is used at the input stage to obtain the difference signal which is further processed to obtain a single digital output word.

The detailed implementation of the constituent components in the SA ADC are discussed in the following sub-sections:

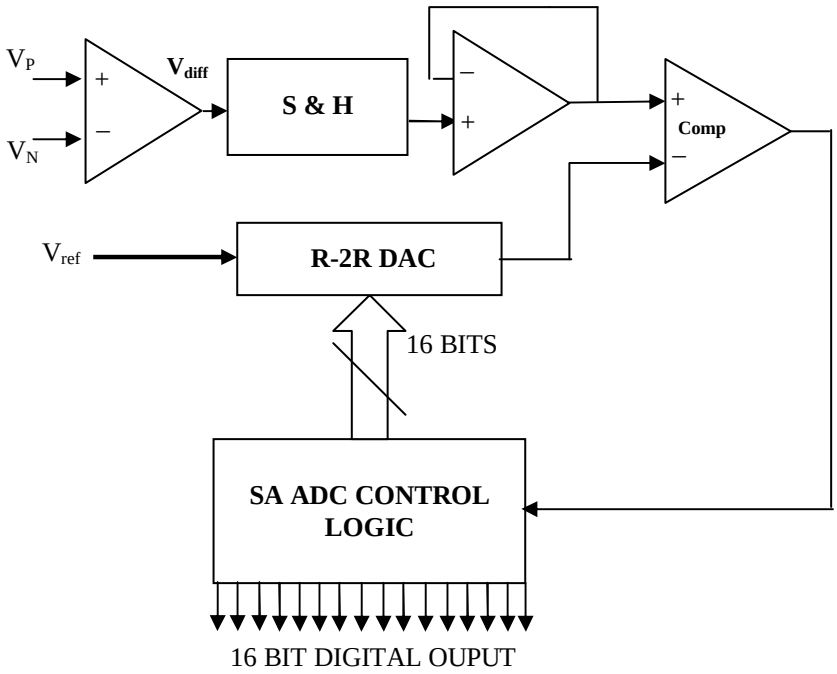

Figure 1: Block Diagram of Successive approximation ADC

2.1. Op-amp used as subtractor:

The designed op-amp employs a 2-stage structure along with a miller capacitance as shown in Fig. 2. It consists of a differential amplifier which hosts a conventional differential input pair, a current mirror and a current source controlled by a bias voltage. The bias voltage is specifically chosen to meet the power requirements. The bias voltage is fully optimised for minimal power consumption. Thus the power consumption of the entire op-amp is very small [3].

The second stage is a amplifier, which is essential to boost up the output swing of the op-amp. The symbolic view with an external resistors connected to form a subtractor is as shown in the Fig. 3, where Vdiff is the difference of the two input analog signal V2 and V1. The generated difference signal is fed to the sample and hold circuit.

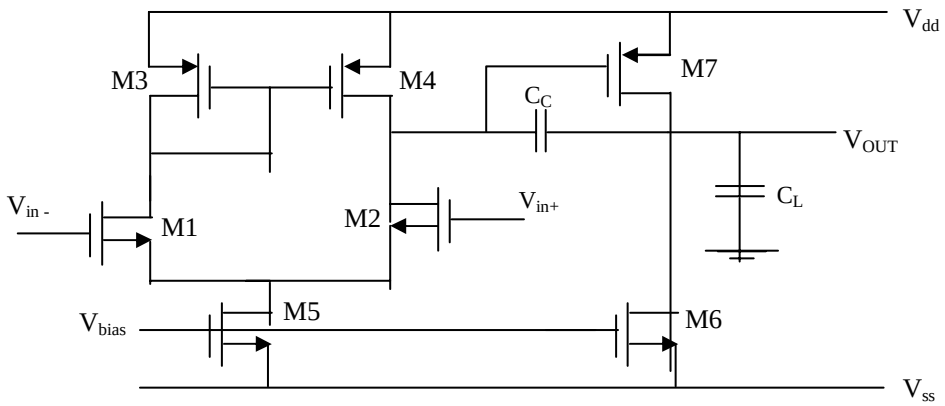

Figure 2: Two stage Miller Compensated Op – amp Schematic

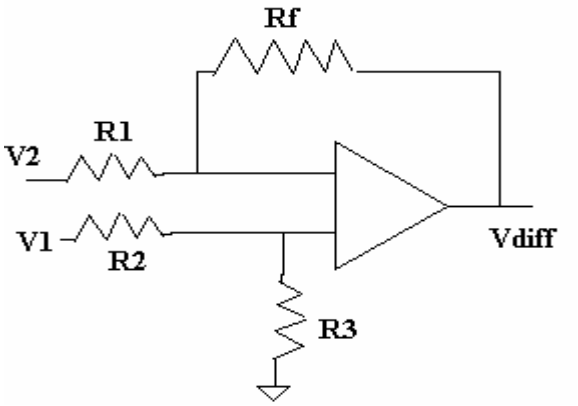

Figure 3: Op-amp used in subtractor mode

2.2. Sample and Hold circuit:

The simplest Sample and hold circuit as shown in Fig.4 employs CMOS switch and sampling capacitor. At a sampling rate of 200Hz and a resolution of 16 bits, a charge injection error was observed which was eliminated by using a dummy switch Fig. 4. The sampling switch adds certain glitch or charges onto the sampling capacitor thus altering the sampled value [4] [5]. The dummy switch is driven by inverted clock which absorbs the charges injected from the sampling switch. Thus channel charge seen at the sample switch, which forms the glitch or charge injection, is compensated by the dummy switch. In the hold time the sampled value held across the capacitor C_h started to die down during the ADC process by which performance of the ADC was limited. It affected the linearity in that the DNL and INL of 0.5 LSB was difficult to achieve. To overcome this, a voltage buffer was placed at the output of the sample and hold circuit as shown in the Fig. 4. By doing this, it was observed that the sampled value which was earlier tapering down was held substantially constant throughout the ADC process.

2.3. Comparator:

A Low power CMOS latch comparator [6] has been employed in this design. The dynamic latch comparator has been modified to reduce power problem by removing the pre-amplifier stage. The comparator also occupies less area and achieve a better resolution around 10μV and have a smaller offset error. The circuit works in two modes; during the clock mode the circuit is connected to the ground by transistors M8 & M9 while M4 & M5 are on and precharge the output to VDD.

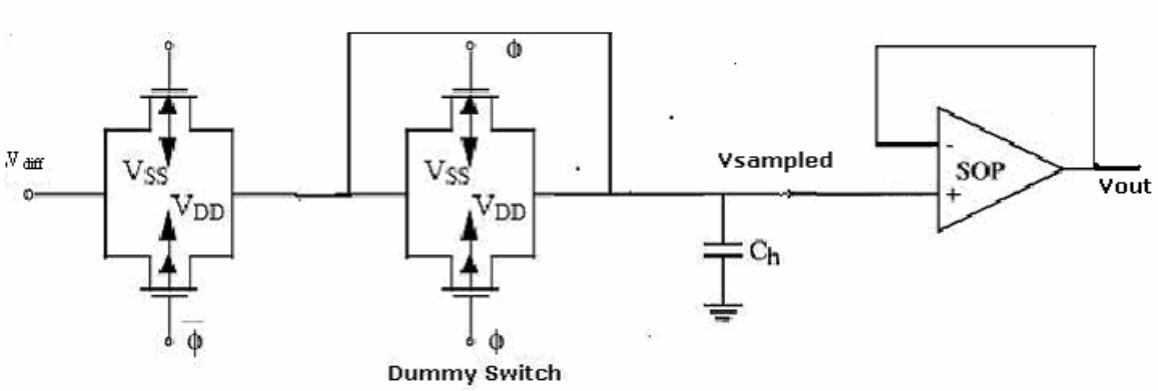

Figure 4: Sample and Hold Circuit with the dummy switch and the output buffer [4].

When the clock goes low the transistor M1 is made on and during this cycle the comparison takes place and only during this phase there is an amount of power consumed. Due to the input parasitic capacitance of the transistors M2 & M3 a load effect was seen at the input of the comparator, which limits the resolution of the comparator to 10 to 12 bits. This will reduce the overall performance of the ADC process. To overcome with this issue the input stage of the comparator was break down to number of transistor in series, thus the parasitic capacitance seen at the input is reduced. The schematic of low power CMOS latch comparator is as shown in the Fig. 5.

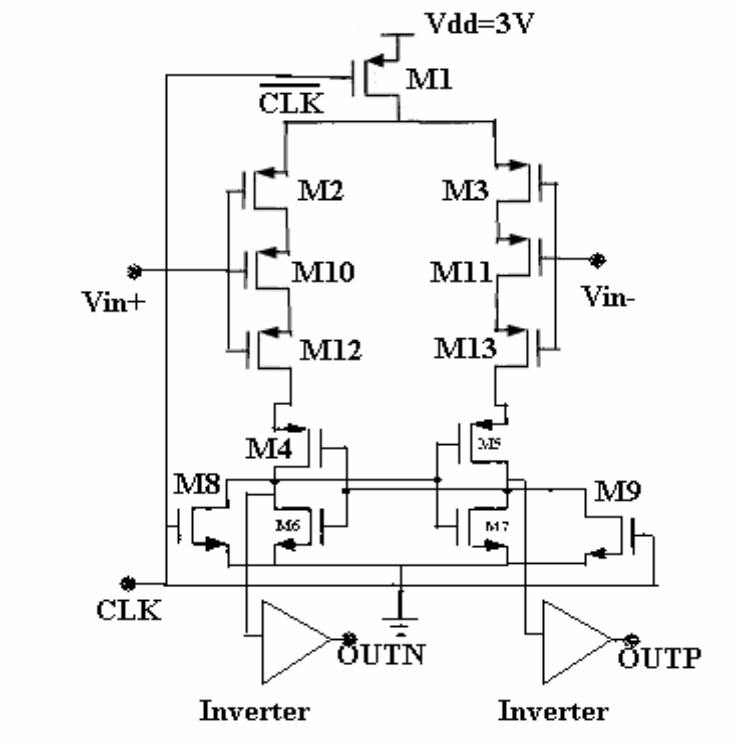

Figure 5: CMOS Latch Comparator

2.4. Digital-to-Analog Converter:

The DAC, employed within the ADC has been designed and optimised for power consumption. A C-2C capacitive DAC was used instead of the conventional binary capacitive DAC to meet the area requirements. As expected the power consumption was found to be very low (in the range of nano-watts). However the resolution of the DAC was insufficient. The design was able to control the accuracy of the ADC only to 12-13 bits. The last 3-4 bits of the digital code generated by the DAC were inaccurate. The DNL and INL are obviously beyond the requirements. The flaw was spotted to be due to the leakage of voltage across the DAC capacitances.

The Fig. 6 shows the drop of voltage across the capacitor with time. This is due to the current leakage through the parasitics [7]. It is almost impossible to eliminate the leakage current, which is very much related to the device physics. The only way to reduce the error is to refresh the capacitor voltage each time the comparison is being made. This would mean that the design would need more switches along with their digital control and an op-amp based structure, which could provide energy to recharge the capacitors.

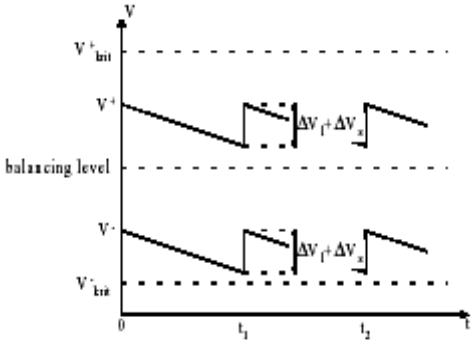

Figure 6: Capacitor leakage effect [7].

Selecting large values for capacitance in the DAC would lower the leakage current. However this would consume large die size. Any small and insignificant leakage in current or drop in the voltage would have been overcome if the working frequency of the ADC was in the range of couple of hundred KHz. However the design requirements needed the ADC to operate at 200Hz, which needs a longer time period clock.

This made the design turn back onto R-2R DAC as shown in Fig.7. The conventional R-2R structure is highly linear. It would hence eradicate the errors associated with linearity. However the problem with the resistive structure is its high power consumption. Hence to reduce power consumption, value of the resistances in the DAC was chosen to be high. To reduce dies size of these high value resistances, implementation was done using bulk type resistors as they have high sheet resistance.

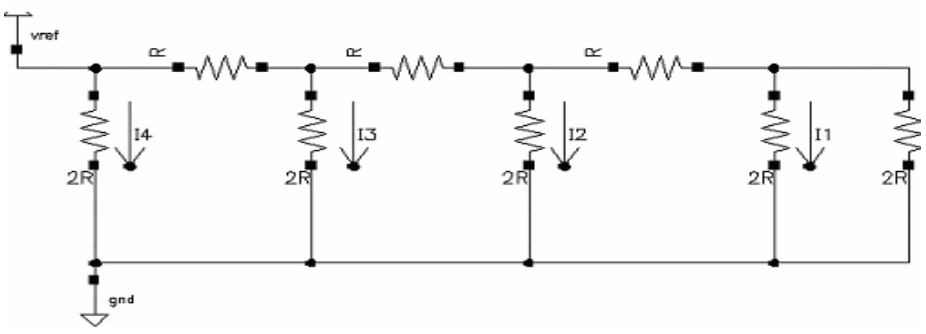

Figure 7: R-2R Ladder Network

However the R-2R DAC has a high gain error [8], due to charge injection from the switch in the sample and hold. If the charge injection were uniform, there would have been a constant offset error, which could be easily eliminated by subtracting the digital equivalent of the analog offset voltage from the digital output. However the charge injection is directly related to the input voltage. Thus the means of reducing this error is to reduce the range of input voltage swing. The current existing input voltage swing was 2Vpeak to peak

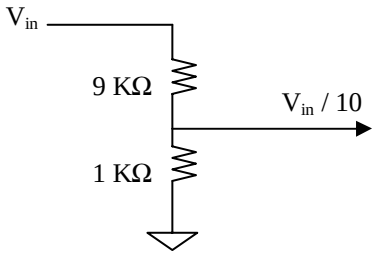

Figure 8: Voltage divider circuit

Thus the design incorporated a small potential divider circuit, which could bring down the input voltage swing effectively before the input was directed to sample and hold circuit. A small circuit Fig.8 was used as a potential divider which ensured that a $1/10^{th}$ of the actual input voltage went to the sample and hold circuitry. The introduction of this section before the sample and hold circuit ensured that the input voltage swing was brought down from 2Vpeak to peak to 0.2V peak to peak. Hence the charge injection variation was drastically brought down. Thus gain slope error was eliminated and the output digital code was thus fine tuned for the required linearity. Apart from eliminating the charge injection, it brought down the reference voltage of the DAC. The reference voltage in the DAC was now 0.2Volts instead of 2Volts. When the reference voltage was reduced by 10 times, the power consumption was reduced nearly 100 times. Effectively the comparator in the circuit had to be responding to a very small difference of 3μvolts while comparing the input voltage and the voltage generated from the DAC. The resolution of the comparator had to be 3μV, which is a very small voltage to be detected. The comparator transistors were varied in their dimensions to get a resolution of 3μvolts.

2.5. Digital Logic:

The digital logic is essential in the SA ADC to control the DAC switches. By switching on and off the various resistance branches, the digital logic thus manipulates the voltages generated by the DAC. The various swicthes are set successively by the comparator output. In each clock, the output comparator sets/resets a swicth starting from the MSB to LSB. A subsequent finite state machine(FSM) using a shift register[9] as shown in Fig.7 is designed which reads the output from the comparator and controls the switches. The figure shown is only for 8-bit ADC, which was extended to 16 bit FSM., also a counter is designed which controls the resetting of all swicthes after 16 comparisons. The counter also generates a signal which controls the sample and hold switch. Thus the FSM is optimised to just 24 flip flops and a digital 5- bit counter stage

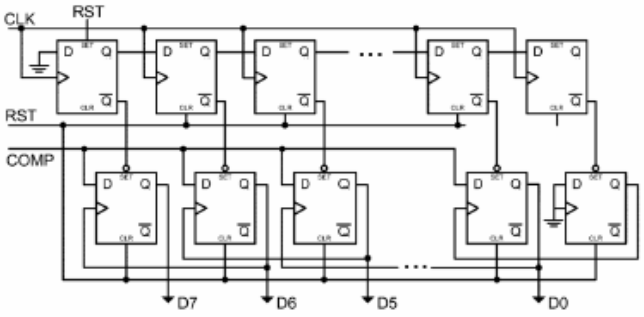

Figure 9: FSM for DAC control

The top set of flip flops act as a shift register, which set the lower flip flop set one after the other starting from the MSB to the LSB. These flip flops inturn control the set or reset of the swicthes of the DAC. These lower set of flip flops later are updated with the comparator output COMP in the next clock and the value is held untill all the 16 comparisons are finished. The flip-flop was required to implement the SA ADC architecture. The main function was to store each bit that was evaluated. Apart from this the flip-flop required additional set and reset functionality. Keeping these points in mind a dynamic C2MOS dynamic D flip-flop was implemented [10].

4. SIMUALTION RESULTS

The designed SA ADC has been implemented in Cadence Analog Artist using 0.18 micron CMOS Process. Figure 9 and Figure 10 present typical plot of Differential Non Linearity (DNL) and Integral Non Linearity (INL) respectively. it is clear that the DNL and INL requirements were met. The DNL and INL were observed to be less than ±0.5LSB.

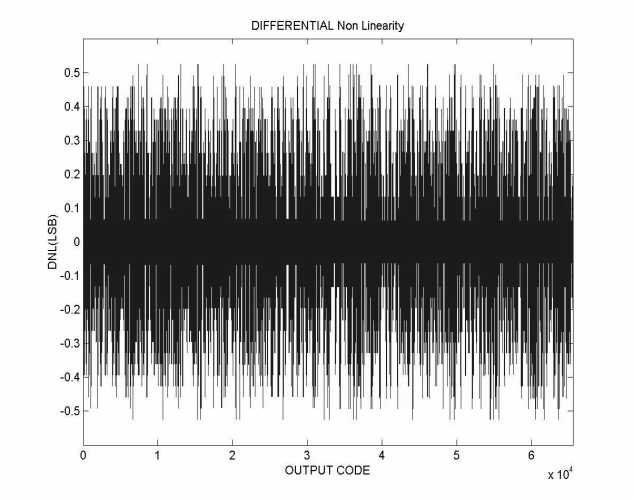

Figure 9: Differential Non Linearity (DNL) error.

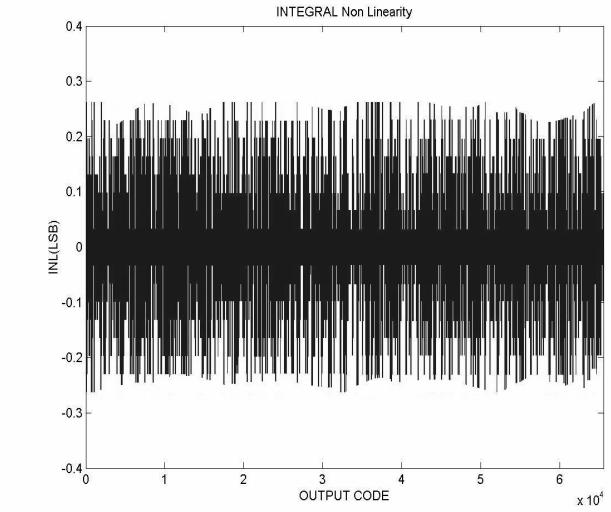

Figure 10: Integral Non Linearity (INL) error

Table 1 summarises the performance of the implemented ADC using the proposed building-block architectures. The ADC consumes a total power of 12µW at an operating speed of 200samples/second. It occupies an area of 0.1mm^2.

Table 1: Performance summary of the designed SA ADC.

Parameter	Value
Resolution	16 bit
Sample rate	200 Samples/s
Area	0.1 mm^2
Analog Power	9.112µWatts
Digital Power	3.08µWatts
Total Power	12.192µWatts
Technology	0.18-micron CMOS
Supply Voltage	3V±20% Volts
Input Range	0-2 Volts
Differential Non - Linearity	≤ ± 0.5 LSB
Integral Non -Linearity	≤ ± 0.5 LSB

5. CONCLUSION

A modified Successive SA ADC architecture has been presented in this paper. The design slightly alters the basic differential SA ADC structure, taking advantage of certain unconventional ideas in order to meet the power and area specifications. The linearity of the SA ADC depends on the linearity of the internal digital-to-analog converter. With the SA converter, the accuracy of using a C-2C DAC limited to 8 to 10 bits. By using R-2R ladder network a 16 bit resolution was obtained but a slope gain error was seen. By scaling the input voltage swing by 10 times, the slope gain error was drastically reduced. With reduction in the gain error the DNL and INL error was limited to ± 0.5 LSB and ± 0.3 LSB. The input stage of the dynamic latched comparator has been modified to reduce the parasitic capacitance, hence a resolution as low as 10µV was achieved. The whole digital core consists of 42 flip-flops. A C^{2}MOS flip-flop has been implemented which gave a reduced transistor count in order to reduce area. The ADC consumes a total power of 12µW at an operating speed of 200samples/second. It occupies an area of 0.1mm^2.

6. REFERENCES

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